



# P67H2-A

Rev : 1.1

ECS  
CONFIDENTIAL

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RD - ELI  
LAYOUT : RITA

NOTE:  
Design by 428971\_428971\_Sugar\_Bay\_and\_BromolowWS\_PDG\_Rev1\_01,  
428880\_428880\_Cougar\_Point\_Desktop\_Ballout\_Mech\_Package\_Revlp0.zip

## REVISION HISTORY:

Rev	Date	Notes
V.A	2010/05/04	Initial version
V.B	2010/06/15	Lucid HYDRA Core
V.1.0	2010/08/13	Integrated Clock Mode
V.1.1	2010/09/07	I-POD Charge Support

## PCB Impedance control

Impedance (OHM)	Trace Width (mil)	(S/W/S)	Trace Length (inch)	Pre-preg	Default
50	4	(16/4/16)	8	1080	TOP BOTTOM
60	5	(20/5/20)	10	2116	INT

1)Circuit type 1

PCB STACK:

Layer 1:TOP

Layer 2:PWR

Layer 3:INT1

Layer 4:INT2

Layer 5:GND

Layer 6:BOTTOM

VCC3 IP

Trace on layer 1

Trace on layer 6

15-R97-011100 PCB M/B.P67H2-A.V1.1  
..W/ECSLOGO...305\*244\*1.6mm.6L..LEADFREE..BLACK..OSP...GE1

ECS

Elitegroup Computer Systems

Title

COVER PAGE

Size

Custom

Document Number

P67H2-A

Rev

1.1

Date:

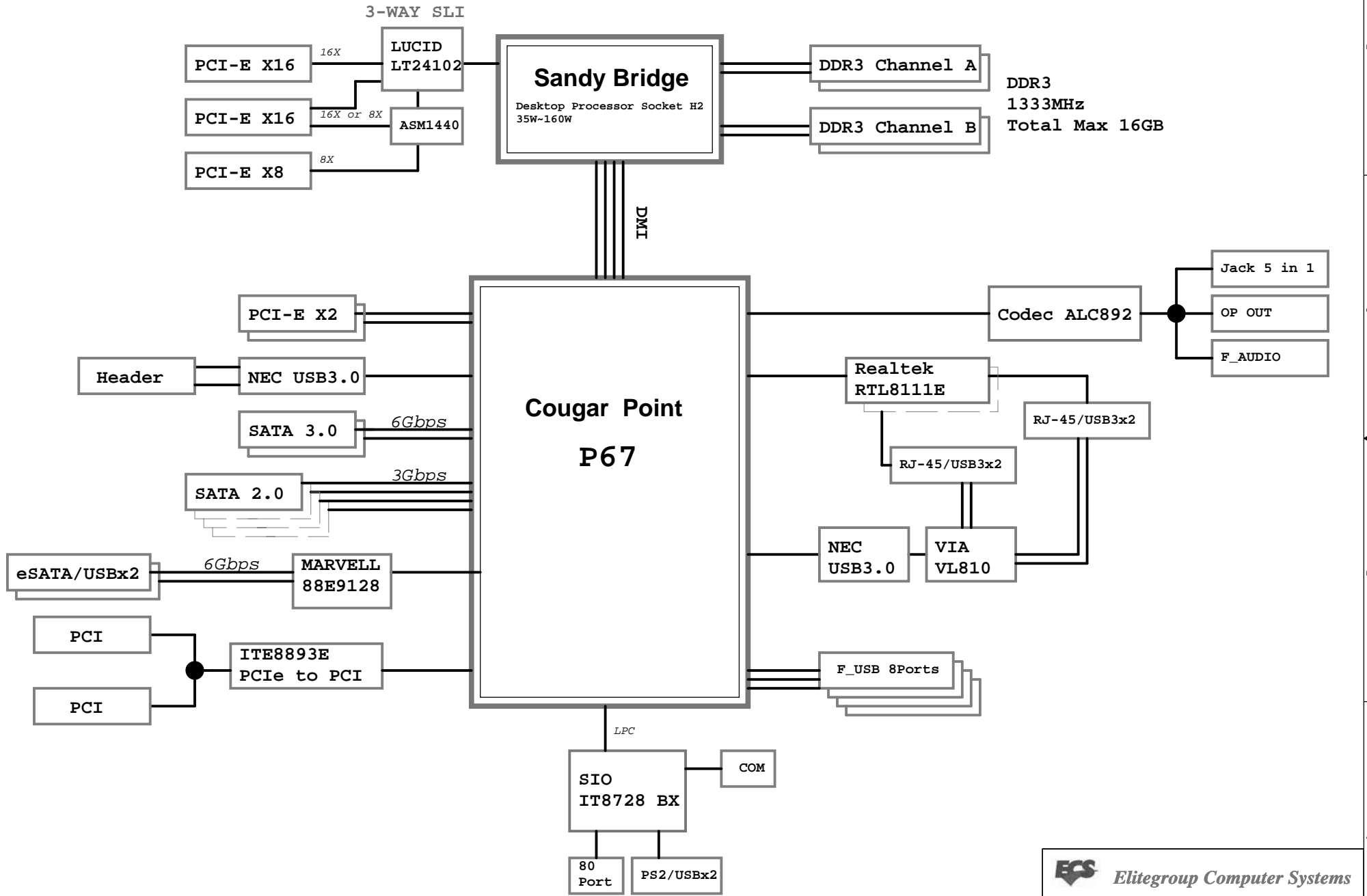
Wednesday, September 15, 2010

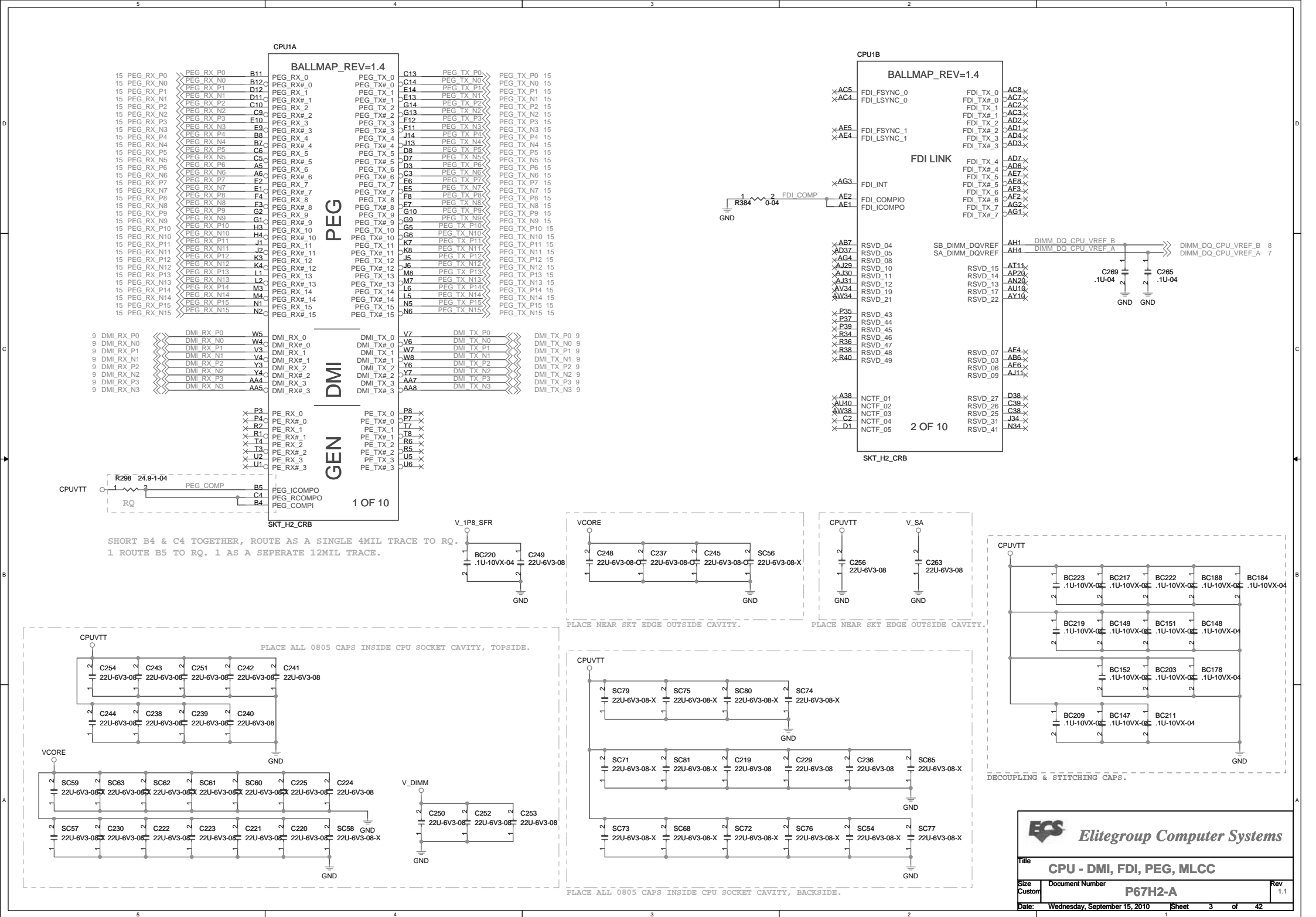
Sheet

1

of

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7 M_DATA_A[0..63]	← M_DATA A[0..63]
7 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
7 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
7 M_MA_A[0..15]	← M_MA A[0..15]
7 M_BS_A[0..2]	← M_BS A[0..2]
7 M_CS_A_L[0..3]	← M_CS A_L[0..3]
7 M_CKE_A[0..3]	← M_CKE A[0..3]
7 M_ODT_A[0..3]	← M_ODT A[0..3]
7 M_CLK_A_P[0..3]	← M_CLK A_P[0..3]
7 M_CLK_A_N[0..3]	← M_CLK A_N[0..3]
7 M_WE_A_L	← M_WE A_L
7 M_CAS_A_L	← M_CAS A_L
7 M_RAS_A_L	← M_RAS A_L

DDR3 CH.A

7,8 DDR3\_DRAMRST\_L ← DDR3\_DRAMRST\_L

8 M_DATA_B[0..63]	← M_DATA B[0..63]
8 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
8 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
8 M_MA_B[0..15]	← M_MA B[0..15]
8 M_BS_B[0..2]	← M_BS B[0..2]
8 M_CS_B_L[0..3]	← M_CS B_L[0..3]
8 M_CKE_B[0..3]	← M_CKE B[0..3]
8 M_ODT_B[0..3]	← M_ODT B[0..3]
8 M_CLK_B_P[0..3]	← M_CLK B_P[0..3]
8 M_CLK_B_N[0..3]	← M_CLK B_N[0..3]
8 M_WE_B_L	← M_WE B_L
8 M_CAS_B_L	← M_CAS B_L
8 M_RAS_B_L	← M_RAS B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_MA_4
M_DATA_A5	AJ1	SA_MA_5
M_DATA_A6	AL2	SA_MA_6
M_DATA_A7	AL1	SA_MA_7
M_DATA_A8	AN1	SA_MA_8
M_DATA_A9	AN4	SA_MA_9
M_DATA_A10	AR3	SA_MA_10
M_DATA_A11	AR4	SA_MA_11
M_DATA_A12	AN2	SA_MA_12
M_DATA_A13	AL1	SA_MA_13
M_DATA_A14	AR2	SA_MA_14
M_DATA_A15	AR1	SA_MA_15
M_DATA_A16	AV2	SA_MA_16
M_DATA_A17	AW3	SA_MA_17
M_DATA_A18	AV5	SA_MA_18
M_DATA_A19	AU2	SA_MA_19
M_DATA_A20	AU3	SA_MA_20
M_DATA_A21	AU5	SA_MA_21
M_DATA_A22	AY5	SA_MA_22
M_DATA_A23	AY7	SA_MA_23
M_DATA_A24	AU7	SA_MA_24
M_DATA_A25	AV9	SA_MA_25
M_DATA_A26	AU9	SA_MA_26
M_DATA_A27	AV7	SA_MA_27
M_DATA_A28	AW7	SA_MA_28
M_DATA_A29	AW8	SA_MA_29
M_DATA_A30	AY9	SA_MA_30
M_DATA_A31	AU35	SA_MA_31
M_DATA_A32	AW37	SA_MA_32
M_DATA_A33	AU39	SA_MA_33
M_DATA_A34	AU36	SA_MA_34
M_DATA_A35	AY36	SA_MA_35
M_DATA_A36	AU38	SA_MA_36
M_DATA_A37	AU37	SA_MA_37
M_DATA_A38	AR40	SA_MA_38
M_DATA_A39	AR37	SA_MA_39
M_DATA_A40	AN35	SA_MA_40
M_DATA_A41	AN37	SA_MA_41
M_DATA_A42	AR39	SA_MA_42
M_DATA_A43	AR38	SA_MA_43
M_DATA_A44	AN39	SA_MA_44
M_DATA_A45	AN40	SA_MA_45
M_DATA_A46	AL40	SA_MA_46
M_DATA_A47	AL37	SA_MA_47
M_DATA_A48	AJ38	SA_MA_48
M_DATA_A49	AJ37	SA_MA_49
M_DATA_A50	AL39	SA_MA_50
M_DATA_A51	AL38	SA_MA_51
M_DATA_A52	AJ39	SA_MA_52
M_DATA_A53	AJ40	SA_MA_53
M_DATA_A54	AG40	SA_MA_54
M_DATA_A55	AG37	SA_MA_55
M_DATA_A56	AE38	SA_MA_56
M_DATA_A57	AE37	SA_MA_57
M_DATA_A58	AG39	SA_MA_58
M_DATA_A59	AG38	SA_MA_59
M_DATA_A60	AE39	SA_MA_60
M_DATA_A61	AE40	SA_MA_61
M_DATA_A62		SA_MA_62
M_DATA_A63		SA_MA_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7
M_DQS_A_N0	AK2	SA_DQS_8
M_DQS_A_N1	AP2	SA_DQS_9
M_DQS_A_N2	AV4	SA_DQS_10
M_DQS_A_N3	AW8	SA_DQS_11
M_DQS_A_N4	AV36	SA_DQS_12
M_DQS_A_N5	AP39	SA_DQS_13
M_DQS_A_N6	AK39	SA_DQS_14
M_DQS_A_N7	AF39	SA_DQS_15

SM\_DRAMRST#

SA\_DQS\_8  
SA\_DQS\_8

SA\_ECC\_CB\_0  
SA\_ECC\_CB\_1  
SA\_ECC\_CB\_2  
SA\_ECC\_CB\_3  
SA\_ECC\_CB\_4  
SA\_ECC\_CB\_5  
SA\_ECC\_CB\_6  
SA\_ECC\_CB\_7

DDR\_0  
3 OF 10

SKT\_H2\_CRB

DDR3 CH.A

## BALLMAP\_REV=1.4

AV27	M_MA_A0
AV24	M_MA_A1
AW24	M_MA_A2
AW23	M_MA_A3
AV23	M_MA_A4
AT24	M_MA_A5
AT23	M_MA_A6
AJ24	M_MA_A7
AV22	M_MA_A8
AT22	M_MA_A9
AV28	M_MA_A10
AJ21	M_MA_A11
AT21	M_MA_A12
AW32	M_MA_A13
AJ20	M_MA_A14
AT20	M_MA_A15
SA_WE#	
SA_CAS#	
SA_RAS#	
SA_BS_0	
SA_BS_1	
SA_BS_2	
SA_CS#_0	
SA_CS#_1	
SA_CS#_2	
SA_CS#_3	

AV19	M_CKE_A0
AT19	M_CKE_A1
AJ18	M_CKE_A2
AV18	M_CKE_A3

AV31	M_ODT_A0
AJ32	M_ODT_A1
AJ30	M_ODT_A2
AW33	M_ODT_A3

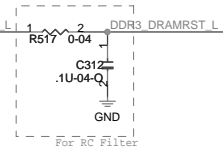
AY25	M_CLK_A_P0
AW25	M_CLK_A_N0
AJ24	M_CLK_A_P1
AJ25	M_CLK_A_N1
AW27	M_CLK_A_P2
AY27	M_CLK_A_N2
AV26	M_CLK_A_P3
AW26	M_CLK_A_N3

AW18DDR3\_DRAMRST\_R\_L

AV13  
AV12

AJ12  
AJ14  
AW13  
AY13  
AJ13  
AJ11  
AY12  
AW12

desktop dosen't support ECC



Pay Attention to This Part!

CPU1D

## BALLMAP\_REV=1.4

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B13	AJ7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B11	AM10	SB_DQ_10
M_DATA_B15	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B8	AM6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B10	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B49	AM31	SB_DQ_49
M_DATA_B50	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B54	AM34	SB_DQ_52
M_DATA_B49	AL31	SB_DQ_53
M_DATA_B53	AM35	SB_DQ_54
M_DATA_B50	AL34	SB_DQ_55
M_DATA_B56	AH35	SB_DQ_56
M_DATA_B57	AH34	SB_DQ_57
M_DATA_B58	AE34	SB_DQ_58
M_DATA_B59	AE35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS_8
M_DQS_B_N1	AL8	SB_DQS_9
M_DQS_B_N2	AP8	SB_DQS_10
M_DQS_B_N3	AN12	SB_DQS_11
M_DQS_B_N4	AN28	SB_DQS_12
M_DQS_B_N5	AR32	SB_DQS_13
M_DQS_B_N6	AM33	SB_DQS_14
M_DQS_B_N7	AG34	SB_DQS_15

SB\_DQS\_8  
SB\_DQS\_8

SB\_ECC\_CB\_0  
SB\_ECC\_CB\_1  
SB\_ECC\_CB\_2  
SB\_ECC\_CB\_3  
SB\_ECC\_CB\_4  
SB\_ECC\_CB\_5  
SB\_ECC\_CB\_6  
SB\_ECC\_CB\_7

DDR\_1  
4 OF 10

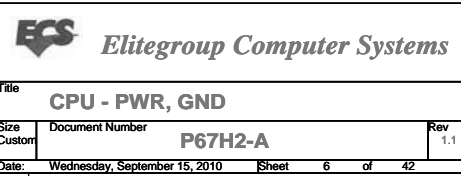
SKT\_H2\_CRB

DDR3 CH.B

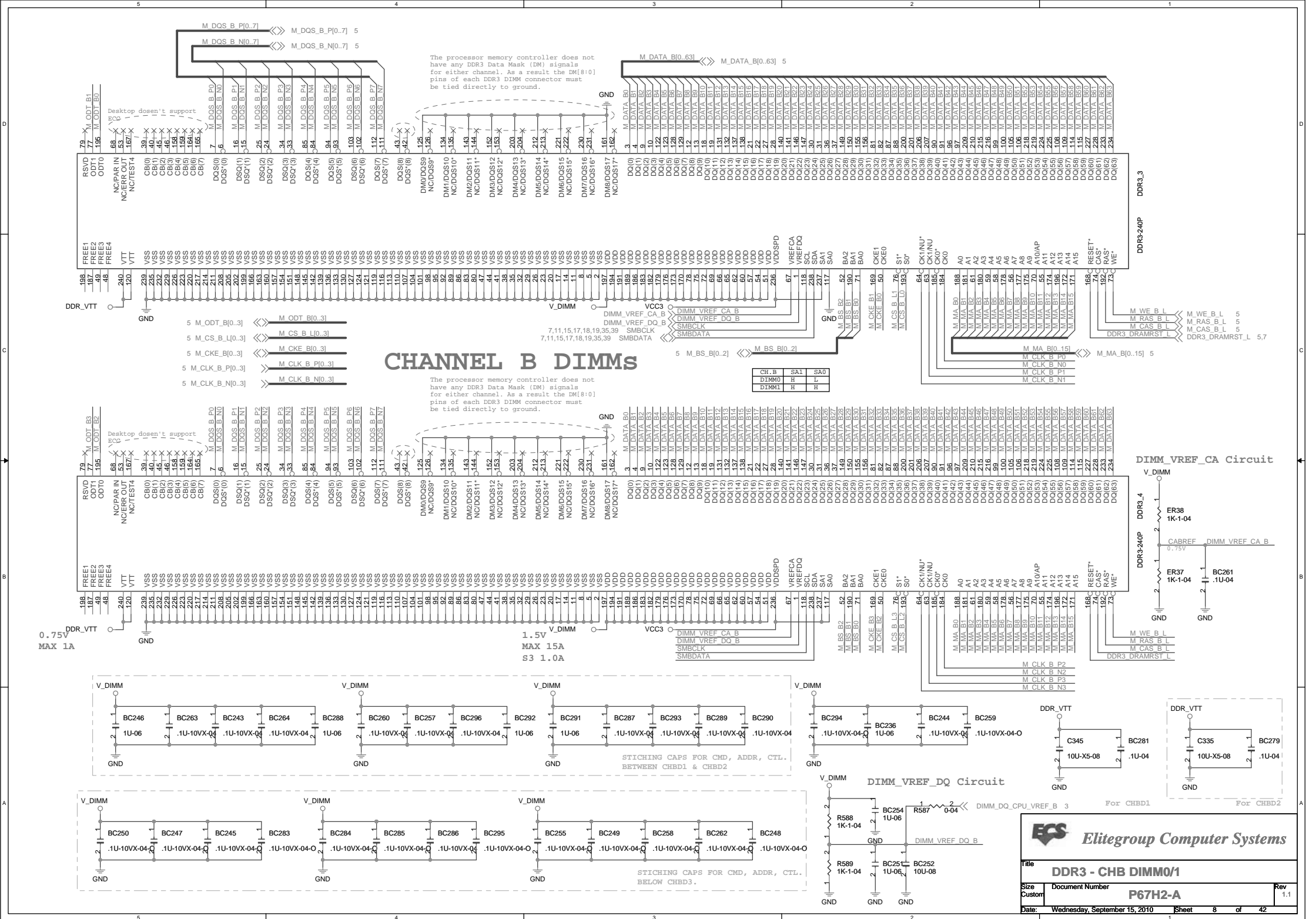


Elitegroup Computer Systems

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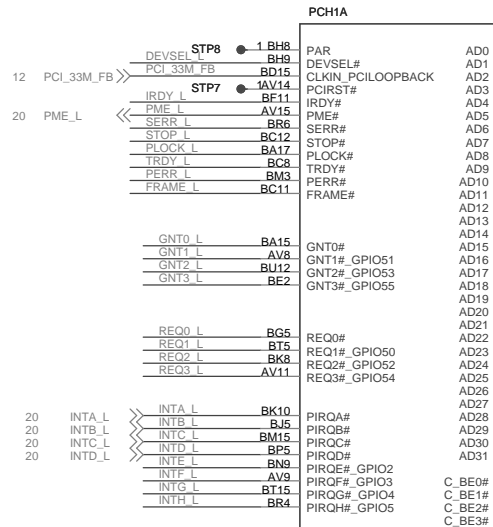








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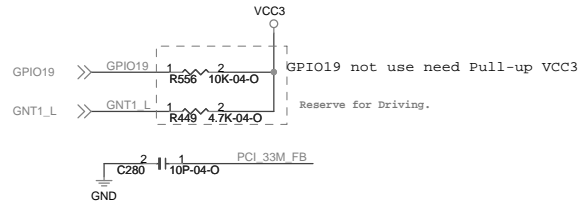
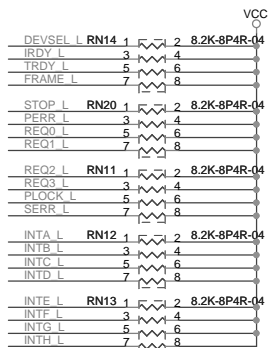


U1CPT

## Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

\* GNT[0..3]#  
GPIO19  
have been internal pull high to +VCC3



PCI

USB3.0

USB3.0

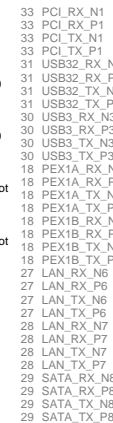
PCIe slot

PCIe slot

LAN1

LAN2

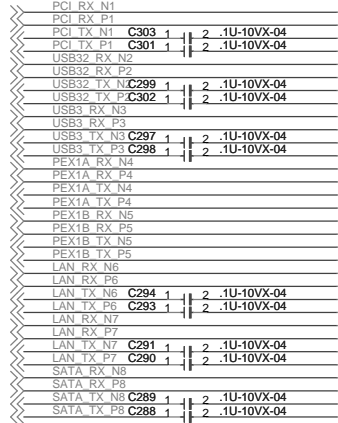
eSATA



V\_1P05\_PCH

Stuff for Integrated Clock Mode

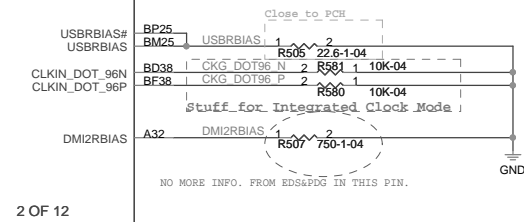
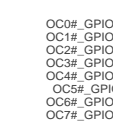
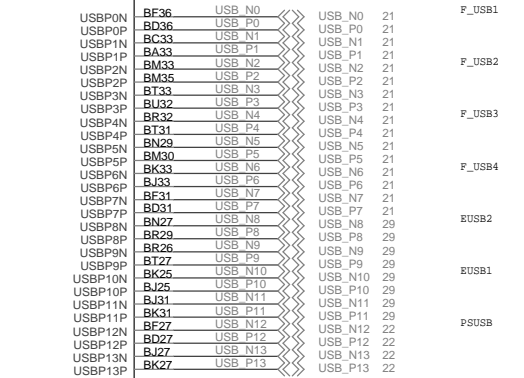
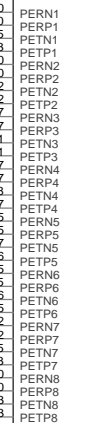
GND 1 R583 2 10K-04  
1 R582 2 10K-04



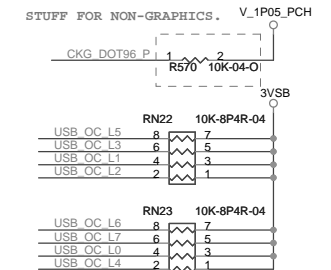
PCH1B



CKG DMI N P33  
CKG DMI P R33



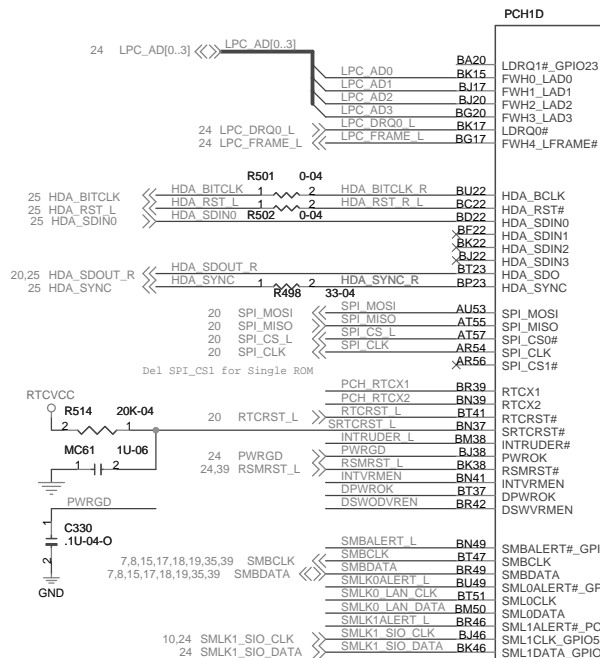
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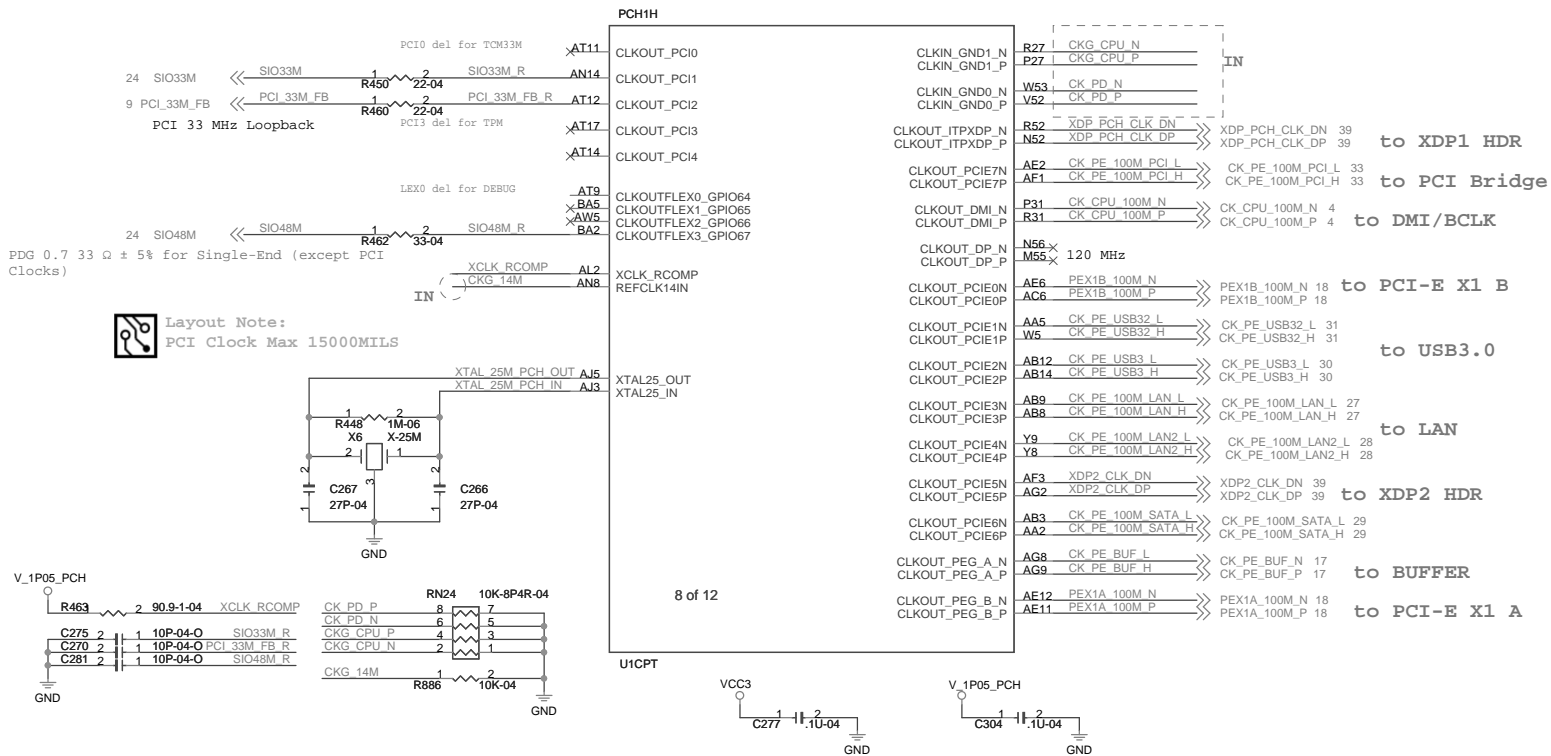


**ECS** Elitegroup Computer Systems

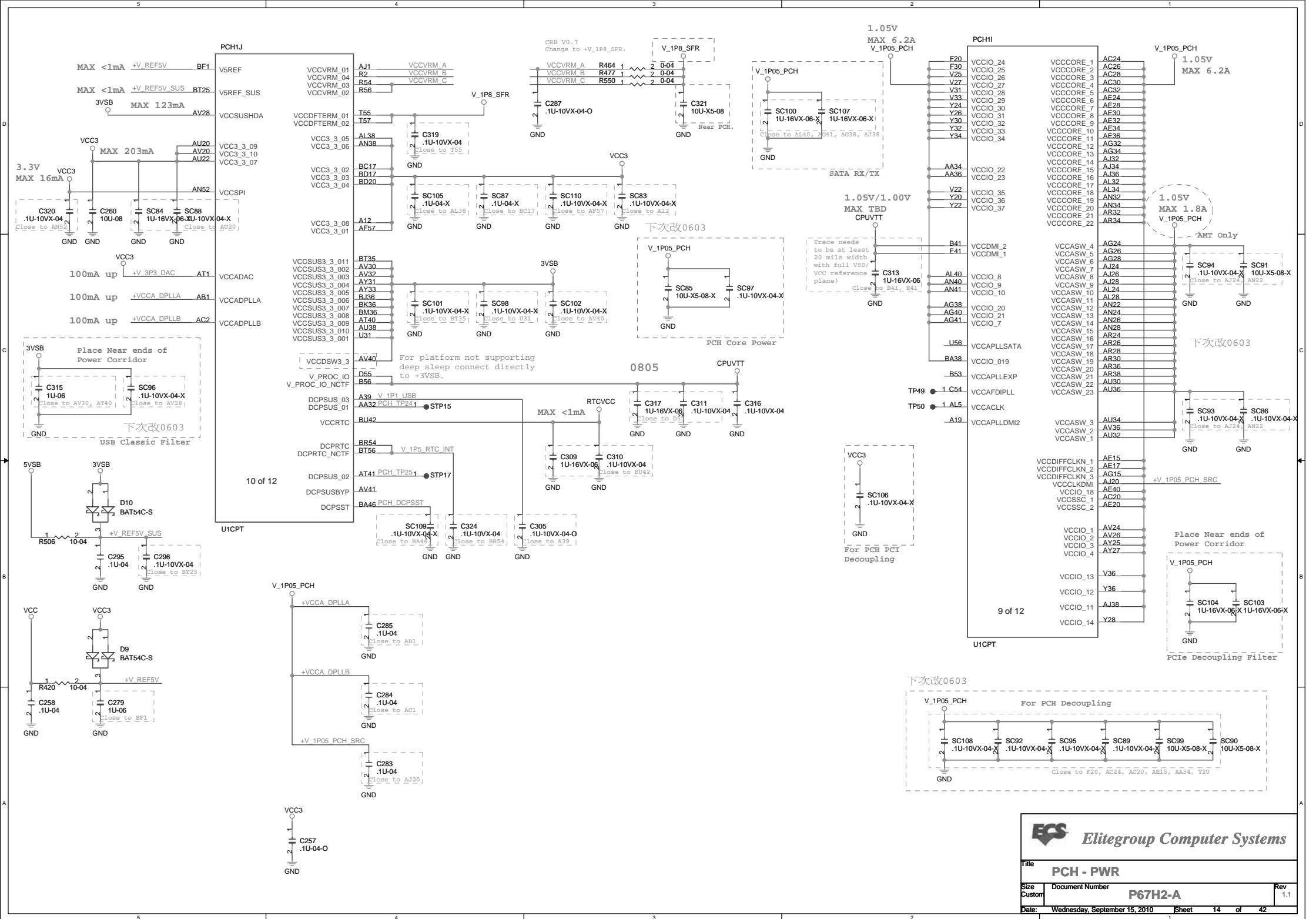
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Size	Document Number	P67H2-A	Rev 1.1
Custom			
Date:	Wednesday, September 15, 2010	Sheet 9	of 42

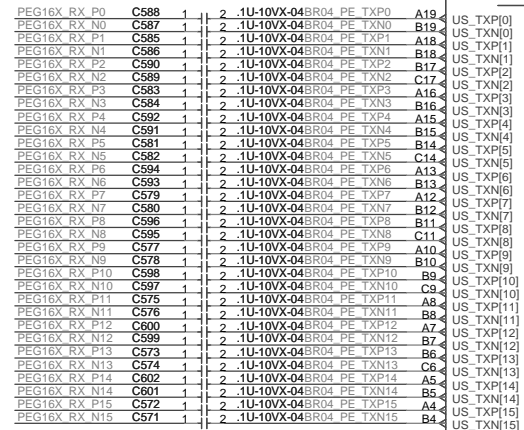
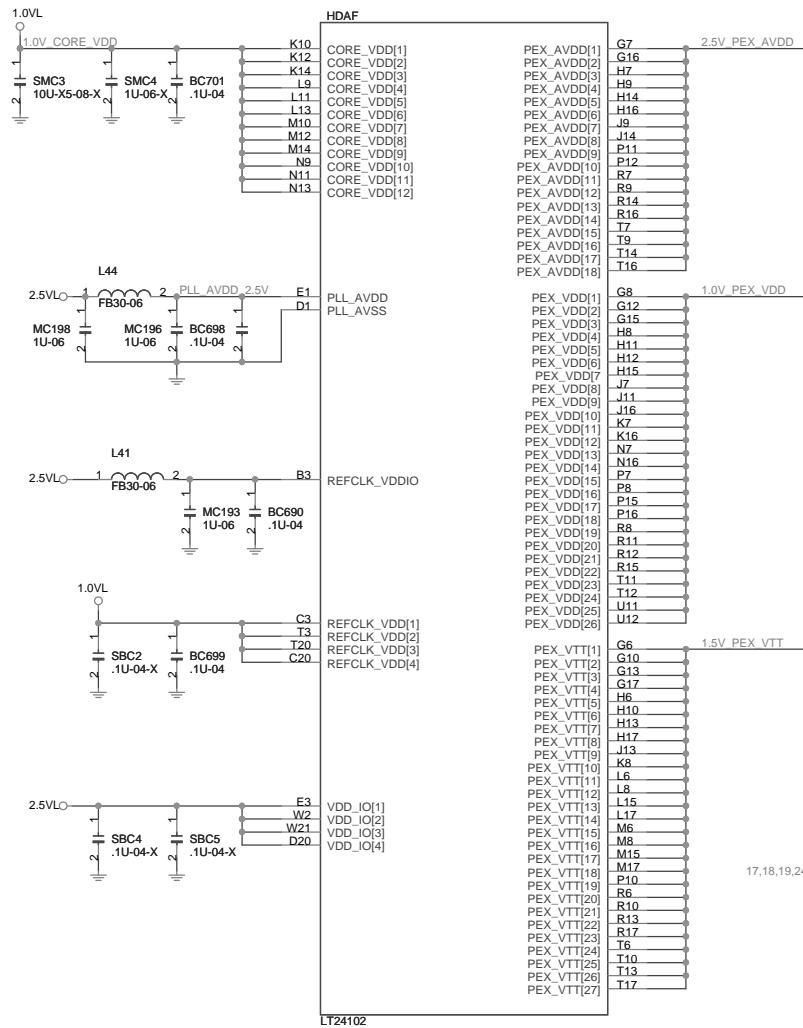












01-201-102720

UPSTREAM TRANSMITTER

UPSTREAM RECEIVER

Power on Reset

ELITEGROUP

I2C\_mode pin="0" reflects I2C mode.  
I2C\_mode pin="1" reflects SMBUS mode.

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

GPIO[3]

10K-04-O

R862

2 SW GPIO5

V22

GPIO[4]

10K-04-O

R866

2 SW GPIO7

Y22

GPIO[7]

10K-04-O

R869

2 SW GPIO8

AA21

GPIO[8]

10K-04-O

R867

2 SW GPIO9

Y21

GPIO[9]

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

GPIO[3]

10K-04-O

R862

2 SW GPIO5

V22

GPIO[4]

10K-04-O

R866

2 SW GPIO7

Y22

GPIO[7]

10K-04-O

R869

2 SW GPIO8

AA21

GPIO[8]

10K-04-O

R867

2 SW GPIO9

Y21

GPIO[9]

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

GPIO[3]

10K-04-O

R862

2 SW GPIO5

V22

GPIO[4]

10K-04-O

R866

2 SW GPIO7

Y22

GPIO[7]

10K-04-O

R869

2 SW GPIO8

AA21

GPIO[8]

10K-04-O

R867

2 SW GPIO9

Y21

GPIO[9]

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

GPIO[3]

10K-04-O

R862

2 SW GPIO5

V22

GPIO[4]

10K-04-O

R866

2 SW GPIO7

Y22

GPIO[7]

10K-04-O

R869

2 SW GPIO8

AA21

GPIO[8]

10K-04-O

R867

2 SW GPIO9

Y21

GPIO[9]

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

GPIO[3]

10K-04-O

R862

2 SW GPIO5

V22

GPIO[4]

10K-04-O

R866

2 SW GPIO7

Y22

GPIO[7]

10K-04-O

R869

2 SW GPIO8

AA21

GPIO[8]

10K-04-O

R867

2 SW GPIO9

Y21

GPIO[9]

2.5V

10K-04-O

R864

2 SW GPIO0

T21

GPIO[0]

10K-04-O

R860

2 SW GPIO1

T19

GPIO[1]

10K-04-O

R865

2 SW GPIO2

U21

GPIO[2]

10K-04-O

R861

2 SW GPIO4

U20

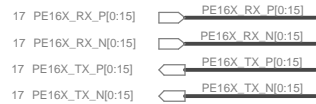
GPIO[3]

10K-04-O

R862

## External Connection

### PCIE16X\_1



### PCIE16X\_2



### PCIE16X\_3



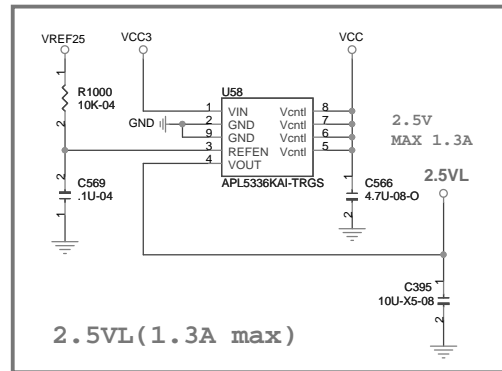
# HYDRA 200

## N-Mode

## A-Mode

## X-Mode

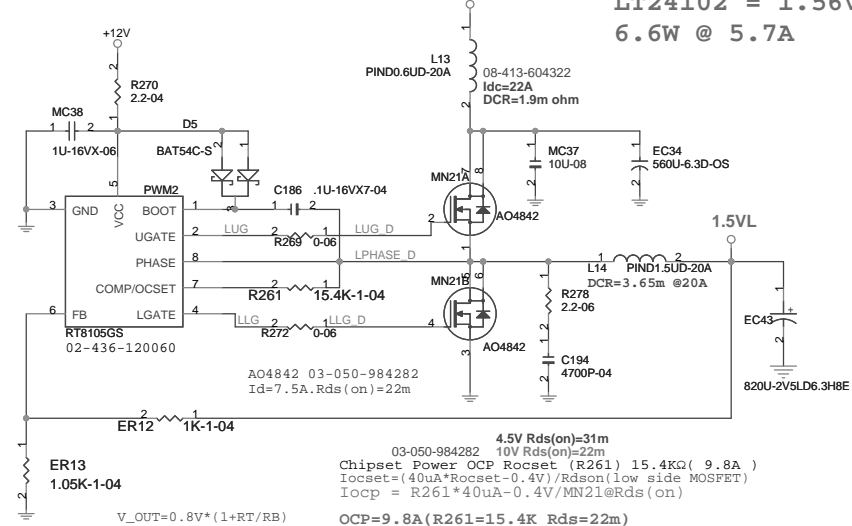
48 x 5 Gbps SERDES lanes,  
a full PCI-Express switch with  
one x16 upstream port,  
two x16 downstream ports  
and an embedded end point.



2.5VL(1.3A max)

## Lucid Power 1.5VL + 1.0VL

LT24102 = 1.56V  
6.6W @ 5.7A





11,18,19,27,28,29,30,31,33 PCIE\_WAKE\_L << PCIE\_WAKE\_L  
7,8,11,15,18,19,35,39 SMBCLK >> SMBCLK  
7,8,11,15,18,19,35,39 SMBDATA << SMBDATA

15,18,19,24,33 SIO\_PCIE16X1\_L >> PEX16\_RST\_L

16 PE16X\_RX\_P[0:15] << PE16X\_RX\_P[0:15]  
16 PE16X\_RX\_N[0:15] << PE16X\_RX\_N[0:15]  
16 PE16X\_TX\_P[0:15] >> PE16X\_TX\_P[0:15]  
16 PE16X\_TX\_N[0:15] >> PE16X\_TX\_N[0:15]

12 CK\_PE\_BUF\_P >> CK\_PE\_BUF\_P  
12 CK\_PE\_BUF\_N >> CK\_PE\_BUF\_N

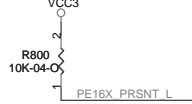
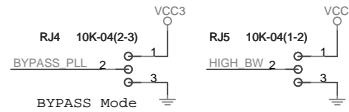
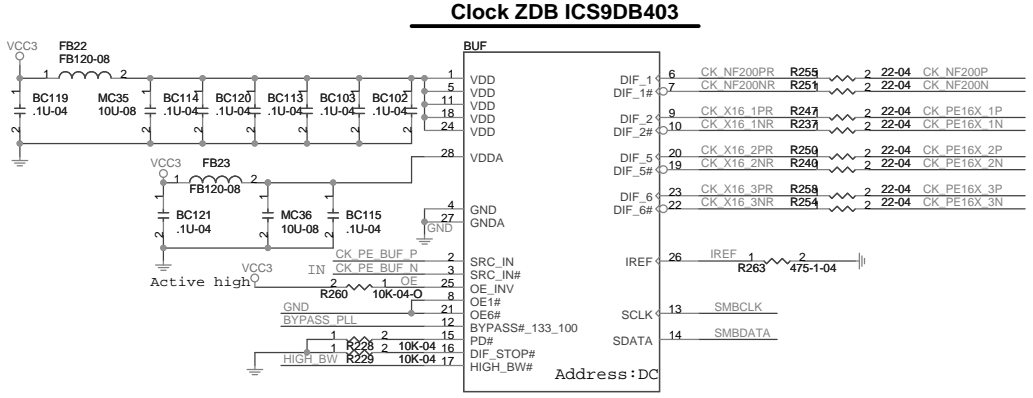
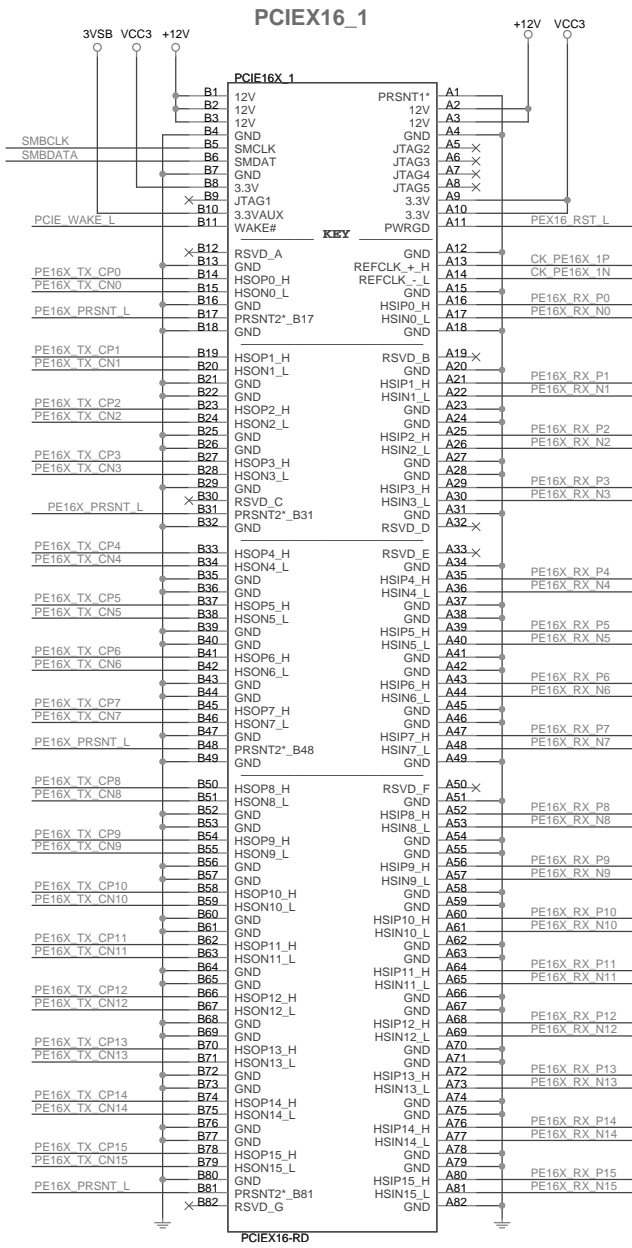
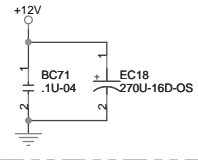
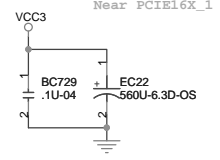
15 CK\_NF200P >> CK\_NF200P  
15 CK\_NF200N >> CK\_NF200N

18 CK\_PE16X\_2P >> CK\_PE16X\_2P  
18 CK\_PE16X\_2N >> CK\_PE16X\_2N

19 CK\_PE16X\_3P >> CK\_PE16X\_3P  
19 CK\_PE16X\_3N >> CK\_PE16X\_3N

PE16X\_TX\_CP0 BC89 1 2 .1U-10VX-04 16X TX P0  
PE16X\_TX\_CP1 BC92 1 2 .1U-10VX-04 16X TX P1  
PE16X\_TX\_CP2 BC96 1 2 .1U-10VX-04 16X TX P2  
PE16X\_TX\_CP3 BC101 1 2 .1U-10VX-04 16X TX P3  
PE16X\_TX\_CP4 BC112 1 2 .1U-10VX-04 16X TX P4  
PE16X\_TX\_CP5 BC118 1 2 .1U-10VX-04 16X TX P5  
PE16X\_TX\_CP6 BC128 1 2 .1U-10VX-04 16X TX P6  
PE16X\_TX\_CP7 BC132 1 2 .1U-10VX-04 16X TX P7  
PE16X\_TX\_CP8 BC136 1 2 .1U-10VX-04 16X TX P8  
PE16X\_TX\_CP9 BC139 1 2 .1U-10VX-04 16X TX P9  
PE16X\_TX\_CP10 BC143 1 2 .1U-10VX-04 16X TX P10  
PE16X\_TX\_CP11 BC154 1 2 .1U-10VX-04 16X TX P11  
PE16X\_TX\_CP12 BC161 1 2 .1U-10VX-04 16X TX P12  
PE16X\_TX\_CP13 BC170 1 2 .1U-10VX-04 16X TX P13  
PE16X\_TX\_CP14 BC181 1 2 .1U-10VX-04 16X TX P14  
PE16X\_TX\_CP15 BC191 1 2 .1U-10VX-04 16X TX P15

PE16X\_TX\_CN0 BC87 1 2 .1U-10VX-04 16X TX N0  
PE16X\_TX\_CN1 BC93 1 2 .1U-10VX-04 16X TX N1  
PE16X\_TX\_CN2 BC98 1 2 .1U-10VX-04 16X TX N2  
PE16X\_TX\_CN3 BC104 1 2 .1U-10VX-04 16X TX N3  
PE16X\_TX\_CN4 BC110 1 2 .1U-10VX-04 16X TX N4  
PE16X\_TX\_CN5 BC123 1 2 .1U-10VX-04 16X TX N5  
PE16X\_TX\_CN6 BC126 1 2 .1U-10VX-04 16X TX N6  
PE16X\_TX\_CN7 BC134 1 2 .1U-10VX-04 16X TX N7  
PE16X\_TX\_CN8 BC137 1 2 .1U-10VX-04 16X TX N8  
PE16X\_TX\_CN9 BC140 1 2 .1U-10VX-04 16X TX N9  
PE16X\_TX\_CN10 BC146 1 2 .1U-10VX-04 16X TX N10  
PE16X\_TX\_CN11 BC157 1 2 .1U-10VX-04 16X TX N11  
PE16X\_TX\_CN12 BC163 1 2 .1U-10VX-04 16X TX N12  
PE16X\_TX\_CN13 BC173 1 2 .1U-10VX-04 16X TX N13  
PE16X\_TX\_CN14 BC185 1 2 .1U-10VX-04 16X TX N14  
PE16X\_TX\_CN15 BC193 1 2 .1U-10VX-04 16X TX N15

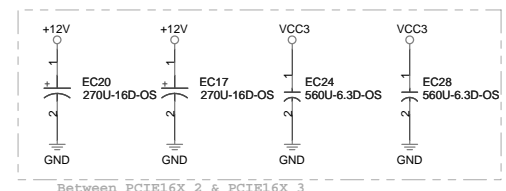


CK\_NF200P R259 2 49.9-1-04  
CK\_NF200N R252 2 49.9-1-04  
CK\_PE16X\_1P R249 2 49.9-1-04  
CK\_PE16X\_1N R238 2 49.9-1-04  
CK\_PE16X\_2P R249 2 49.9-1-04  
CK\_PE16X\_2N R239 2 49.9-1-04  
CK\_PE16X\_3P R251 2 49.9-1-04  
CK\_PE16X\_3N R253 2 49.9-1-04



## External Connection

16 EXP_A_TX_DN[8..15]		<u>EXP A TX DN[8..15]</u>
16 EXP_A_TX_DP[8..15]		<u>EXP A TX DP[8..15]</u>
16 EXP_A_RX_DN[8..15]		<u>EXP A RX DN[8..15]</u>
16 EXP_A_RX_DP[8..15]		<u>EXP A RX DP[8..15]</u>
18 A_EXP_A_TX_DN[8..15]		<u>A EXP A TX DN[8..15]</u>
18 A_EXP_A_TX_DP[8..15]		<u>A EXP A TX DP[8..15]</u>
18 A_EXP_A_RX_DN[8..15]		<u>A EXP A RX DN[8..15]</u>
18 A_EXP_A_RX_DP[8..15]		<u>A EXP A RX DP[8..15]</u>
17 CK_PE16X_3N		<u>CK 16P B DN</u>
17 CK_PE16X_3P		<u>CK 16P B DP</u>
15,17,18,24,33 SIO_PCIEST1_1L		<u>PEX16 RST L</u>
11,17,18,27,28,29,30,31 PCIE_WAKE_L		<u>PCIE WAKE L</u>
7,8,11,15,17,18,35,39 SMBCLK		<u>SMBCLK</u>
7,8,11,15,17,18,35,39 SMBDATA		<u>SMBDATA</u>
15 EXP_B_PRSNT_L		<u>DUAL X8 Enable</u>



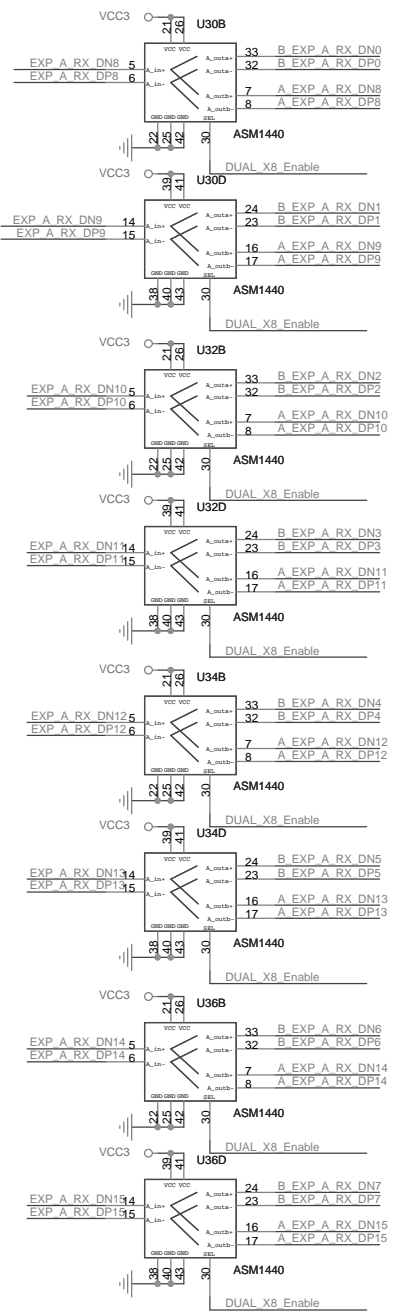
B EXP A TXP 4 C BC109	1	2	.1U-10VX-04	EXP A TX DP4
B EXP A TXN 4 C BC111	1	2	.1U-10VX-04	EXP A TX DN4

B EXP A TXP 5 C BC117 1 2 .1U-10VX-04 EXP A TX DP5  
B EXP A TYN 5 C BC122 1 2 .1U-10VX-04 EXP A TX DN5

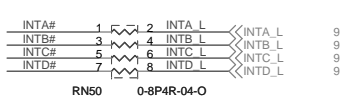
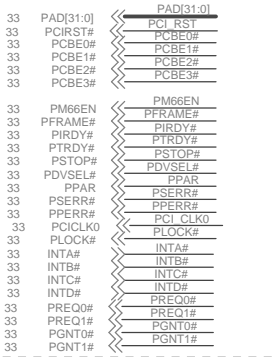
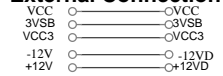
B EXP A TXP 6 C BC125 1 | 2 .1U-10VX-04 EXP A TX DP6

B\_EXP\_A\_TXP\_7\_C BC131 1 11 2 .1U-10VX-04 EXP\_A\_TX\_DP7

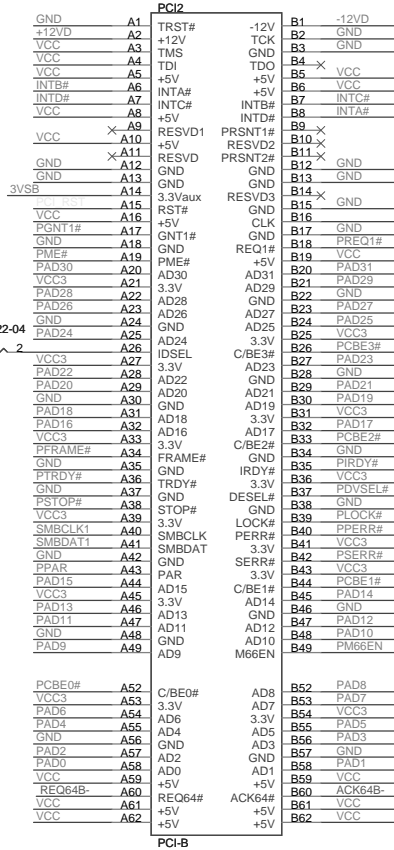
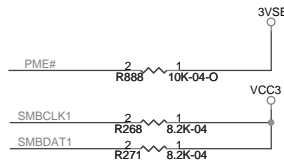
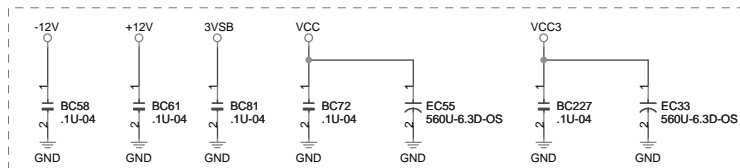
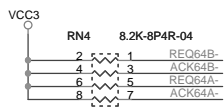
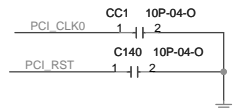
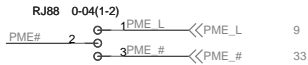
ASM1440 bypass Cap  
每組三顆



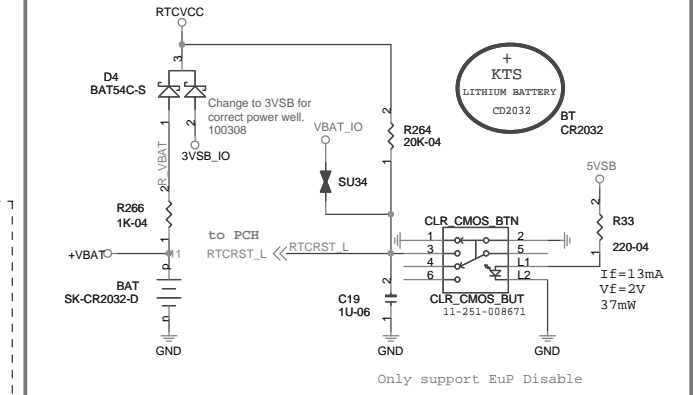
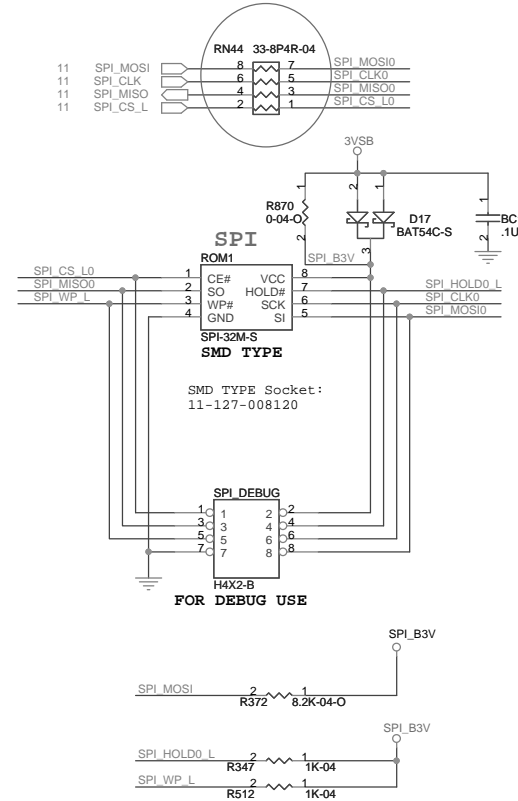
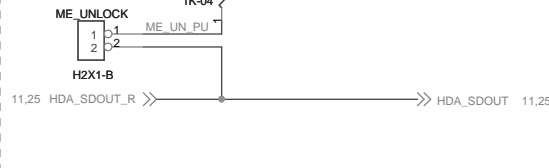
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SLOT - PCIE16X_3, PCIE SW			
Size	Document Number	Rev	
Custom	P67H2-A	1.1	
Date:	Wednesday, September 15, 2010	Sheet	19 of 42

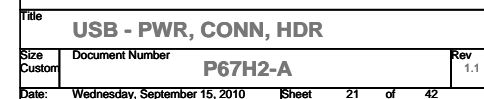


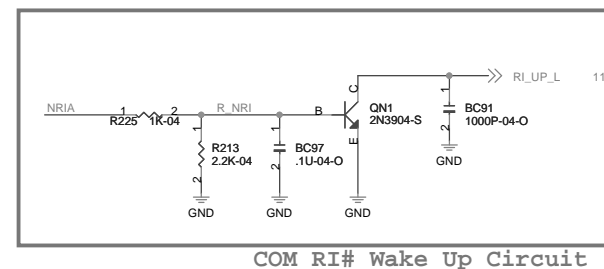
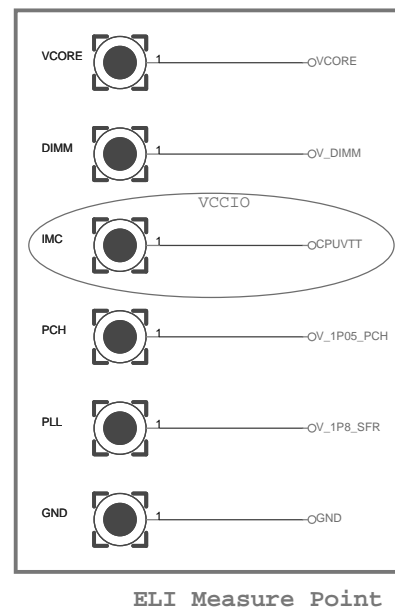
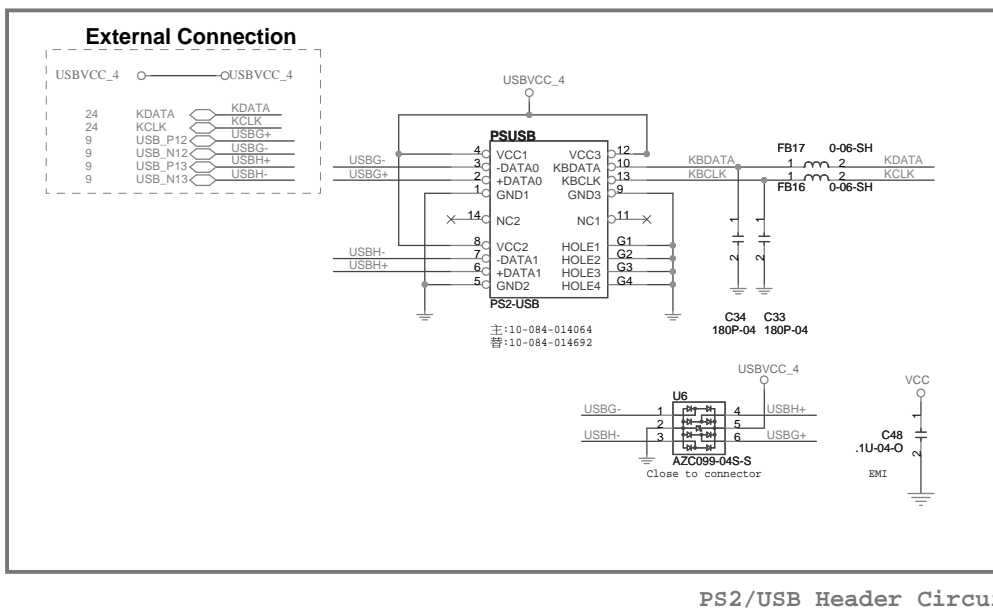
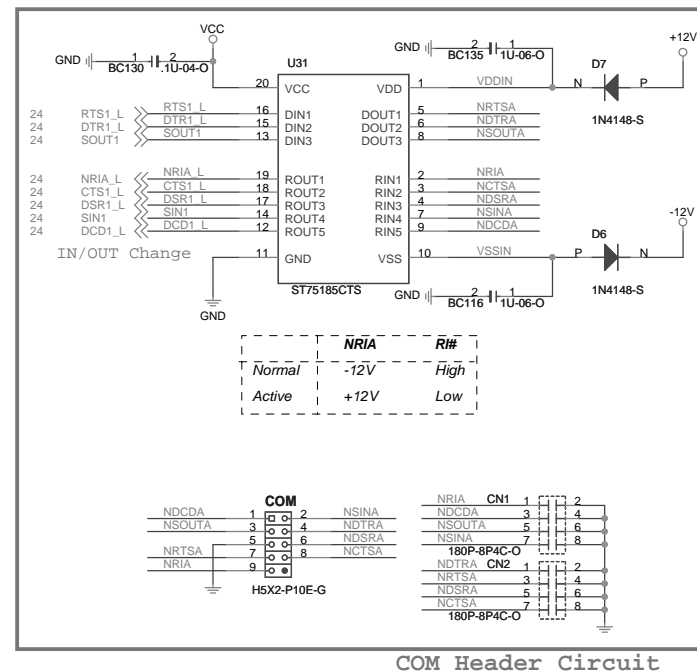
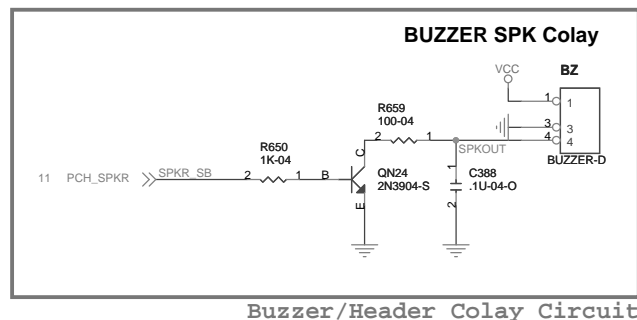
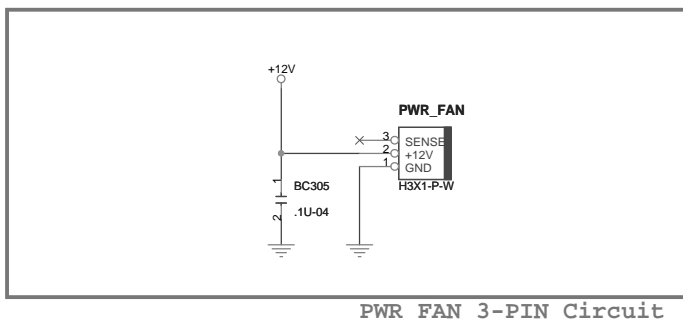
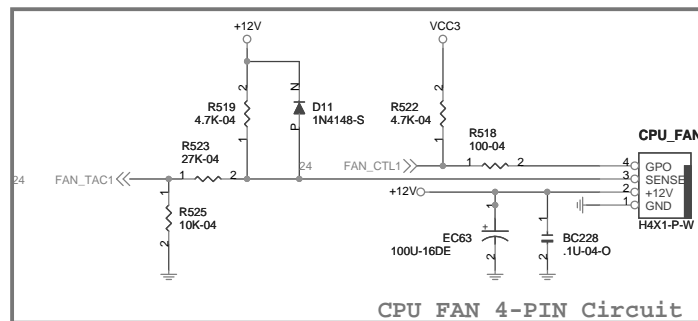
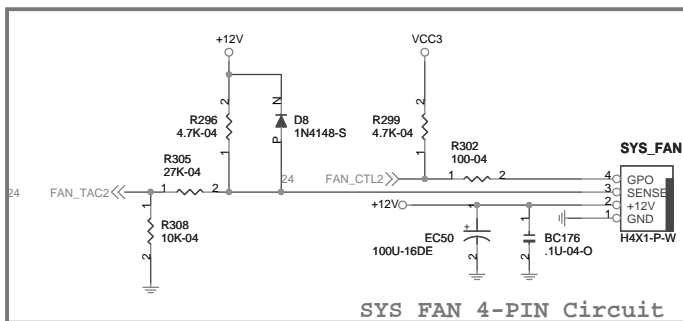
```
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A
```

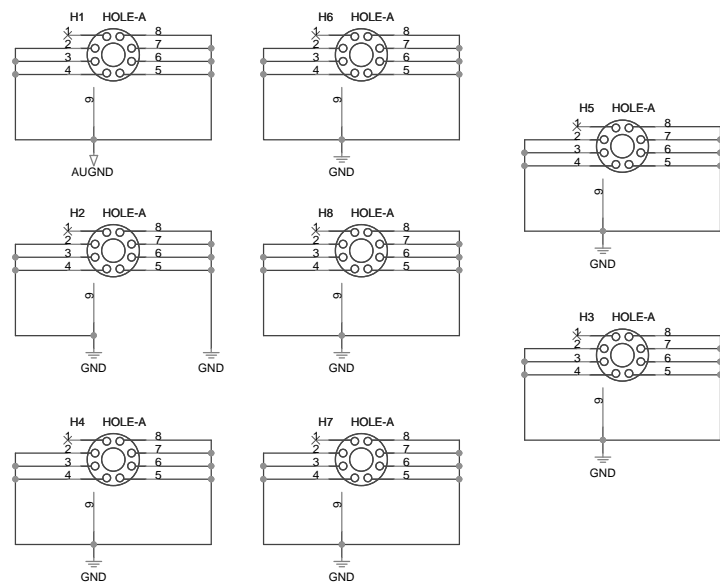
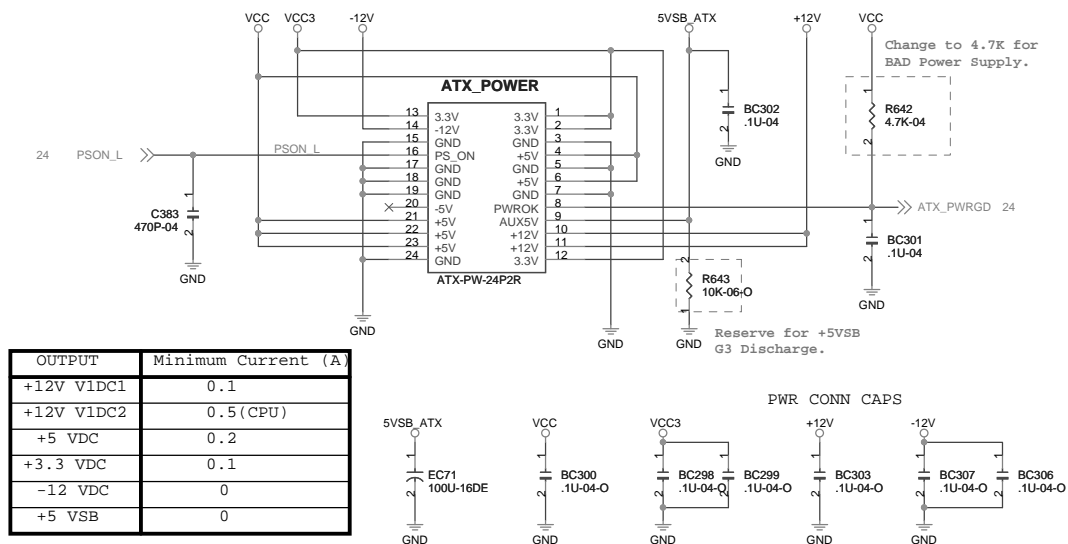


	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

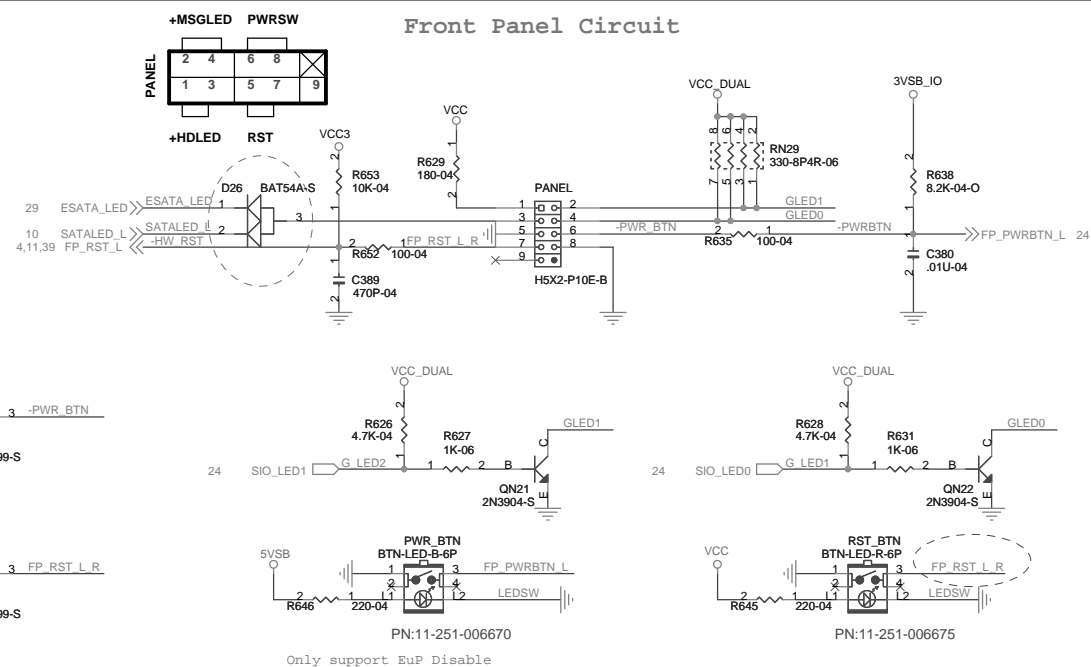
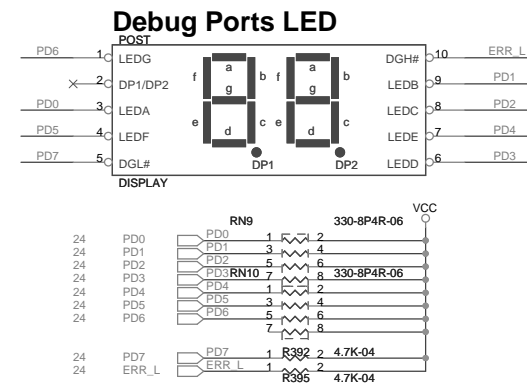








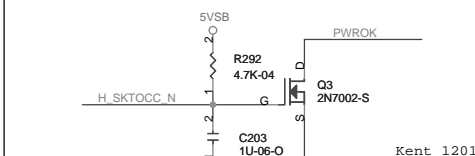
2-Pin Single color LED	
S0	Steady Green
S1,S3	LED-blinking
S4,S5	Off



11	LPC_PME_L		LPCPME_L	LPC
11	LPC_DR00_L		-LPC_DR00	
11	LPC_FRAME_L		-LPC_FRAME	
11	LPC_AD[0..3]		-L_AD[0..3]	
22	RTS1_L		-RTSA	
22	DSR1_L		-DSRA	
22	SOUT1_L		-RXDA	
22	SIN1_L		-DTRA	
22	DTR1_L		-DCDA	
22	DCD1_L		-RI	
22	NRIA_L		-CTSA	COM
22	CTS1_L			
11,39	RSMRST_L		RSMRST_N	
23	FP_PWRBTN		-PANSHW	
11,39	SIO_PWRBTN_L		-PWWRON	
4,11,21,34	SIO_PICRST3_L		-SLP3	
11,21	SLP4_L		-SLP4	
23	PSON_L		-ATX_PSON SIO	
23	ATX_PWRGD		ATX_PWRGD	
11	PWRGD		PWRGD	
11,39	PCH_PLTRST_L		PLTRST_L	
17,18,19,33	SIO_PCIRST1_L		-PCI_RSTY	
4,29	SIO_PCIRST2_L		-PCIE_RSTY	
27,28,30,31	SIO_PCIRST3_L		SIO_PCIRST3_L	
10	SST_CTL		SST_CTL	
10	KBRST_L		-K8_RST	
10	A20GATE		A20GATE_L	
10	SER_IRQ		SERIRQ	
35	3VSB5W		-3VSB5W	
4	PECI		PECI	RST
22	FAN_TAC1		CFAN_TAC1	
22	FAN_CTL1		CFAN_TAC2	
22	FAN_TAC2		CFAN_PWM2	
22	FAN_CTL2		CFAN_PWM2	
23	SIO_LED1		G_LED1	
23	SIO_LED0		G_LED2	
22	CKLK		CKLK	
22	KDATA		KDATA	
32	RST		RST	
12	SIO33M		SIO_PCLK	80-Pin
12	SIO48M		SIO_CLK48	
4,37	H_SKT0CC_L		H_SKT0CC_N	
10,11	SMCLK1_SIO_CLK		SMCLK1	
11	SMCLK1_SIO_DATA		SMCLK1DATA	
10	THERMAL_ALERT		PCH_THRM_L	
34	PCH_GP24		PCH_GP24	
34	PCH_GP25		PCH_GP25	
34	PLL_GP26		PLL_GP26	
34	PLL_GP27		PLL_GP27	
21	5VSB_CTRL		5VSB_CTRL	80-Pin
23	PD0		PD0	
23	PD1		PD1	
23	PD2		PD2	
23	PD3		PD3	
23	PD4		PD4	
23	PD5		PD5	
23	PD6		PD6	
23	PD7		PD7	80-Pin
23	ERR_L		ERR_L	



## Thermal and Voltage Monitor



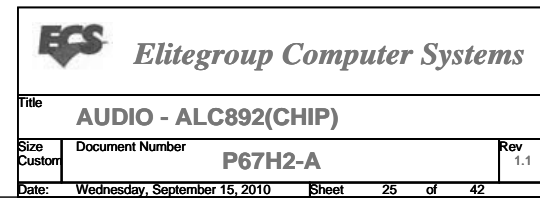
Title			
SIO - ITE8728			
Size Custom	Document Number		Rev
	P67H2-A		1.1
Date:	Wednesday, September 15, 2010	Sheet	24 of 42



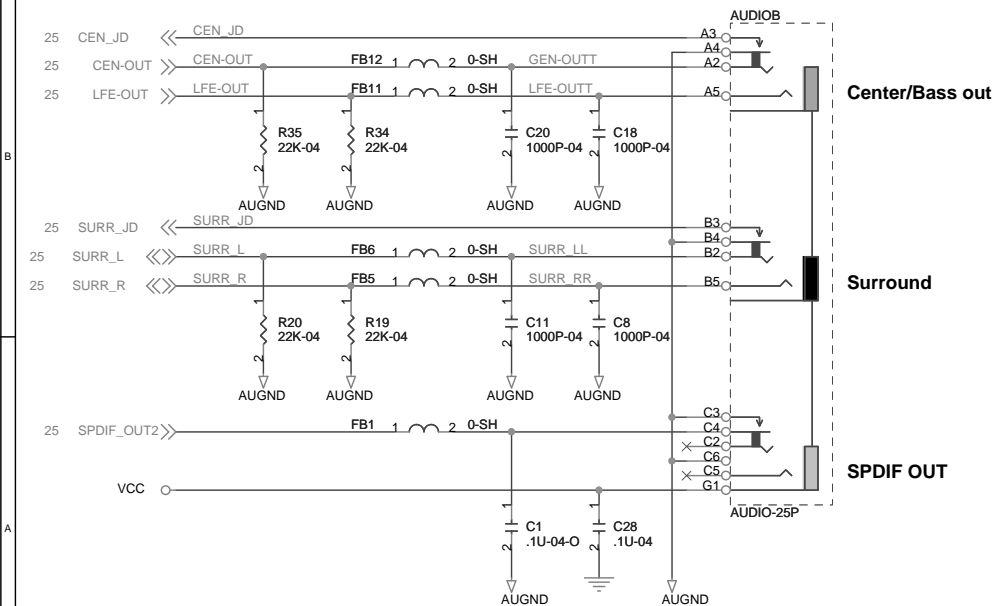
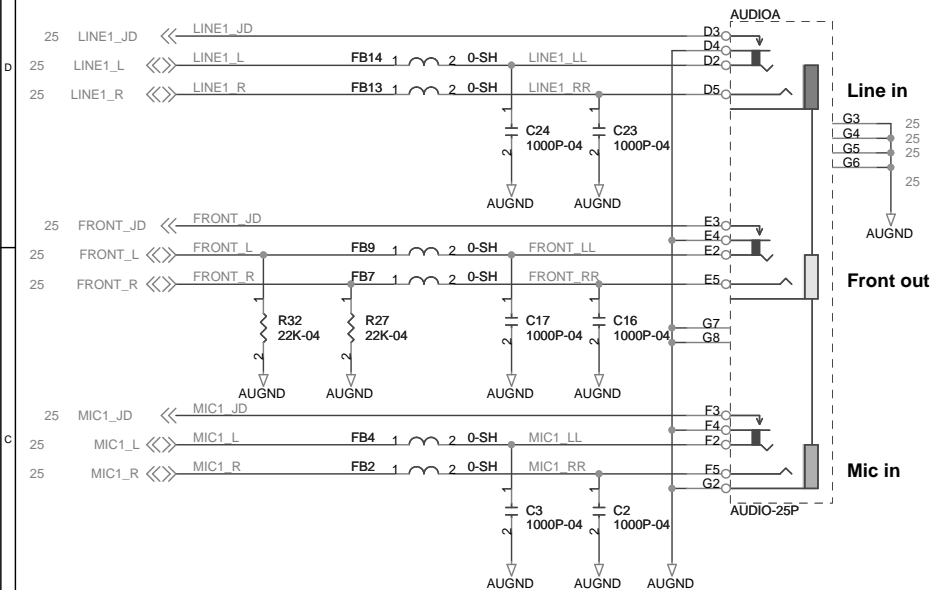
Timing diagram showing the relationship between HDA signals and 5VSB power rail transitions. The signals are:

- 11 HDA\_RST\_L
- 11 HDA\_BITCLK
- 11 HDA\_SYNC
- 11 HDA\_SDINO
- 11,20 HDA\_SDOUT

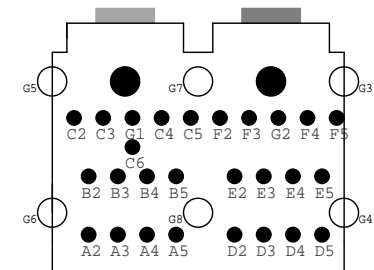
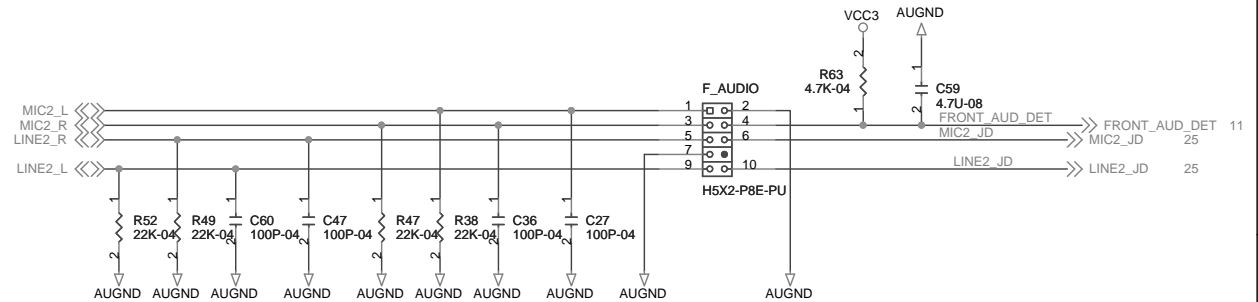
The signals are shown relative to 5VSB power rail transitions, with 5VSB transitions marked by circles and lines. The signals are labeled with their respective names and values: RST, BIT CLK, SYNC, SDATA\_IN, and SDATA\_OUT.



## REAR AUDIO

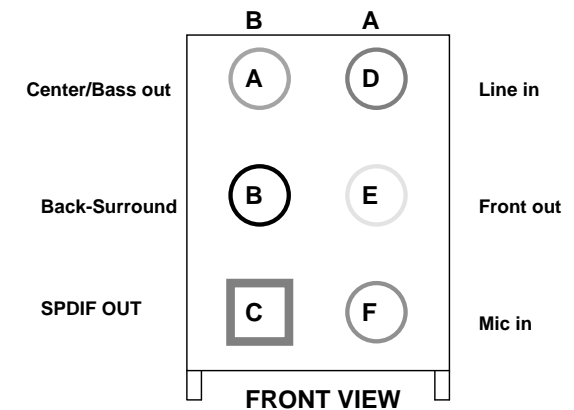
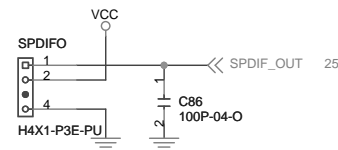


## FRONT AUDIO



**TOP VIEW**

## SPDIF OUT



## Elitegroup Computer Systems

Title	AUDIO - ALC892(PANEL)
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Size Custom	Document Number <b>P67H2-A</b>	Rev 1.1
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Date: Wednesday, September 15, 2010 Sheet 26 of 42



## External Connection

**External Connection**

3VSB ○ ○ 3VSB  
 VCC3 ○ ○ VCC3  
 AUGND2 ◁ ▷ AUGND2

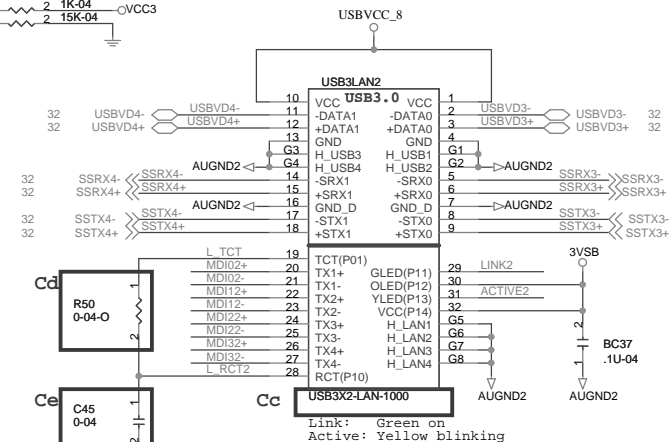
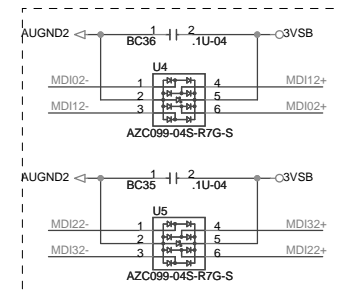
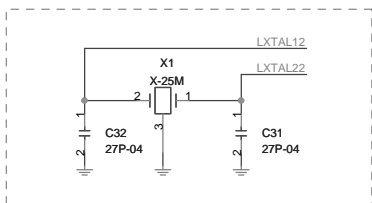
11, 17, 18, 19, 27, 29, 30, 31, 33 PCIE\_WAKE\_L >> PCIE\_WAKE\_UP2-  
 24, 27, 30, 31 SIO\_PCIRST3\_L >> PCIE\_LAN\_RST2-

9 LAN\_TX\_P7 >> LAN\_HSP2  
 9 LAN\_TX\_N7 >> LAN\_HSN2

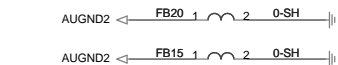
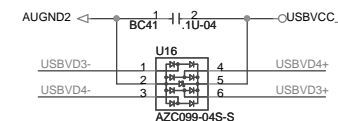
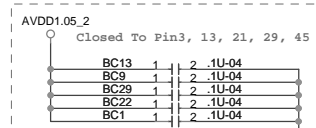
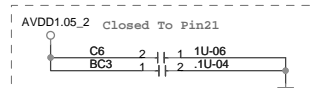
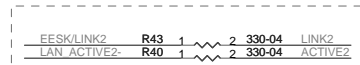
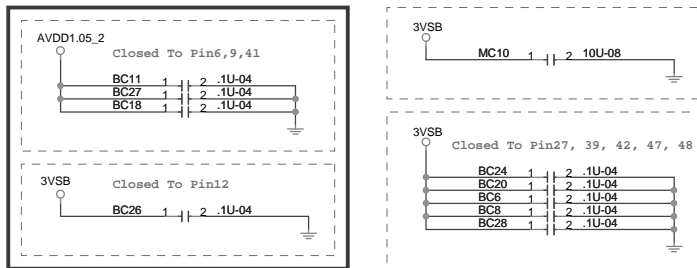
12 CK\_PE\_100M\_LAN2\_H >> CK\_PE\_LANP2  
 12 CK\_PE\_100M\_LAN2\_L >> CK\_PE\_LANN2

9 LAN\_RX\_P7 >> LAN\_HSP2  
 9 LAN\_RX\_N7 >> LAN\_HSN2

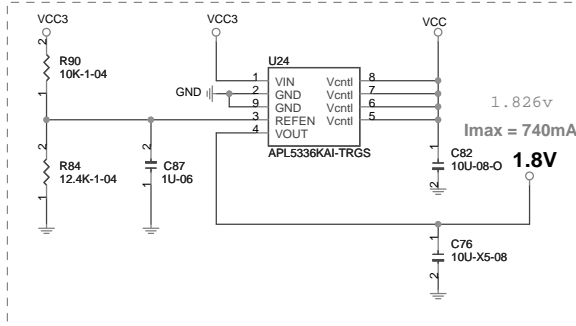
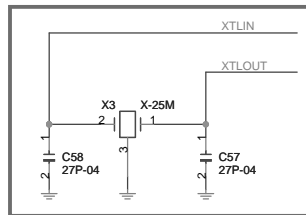
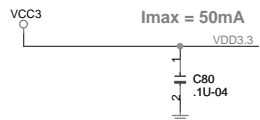
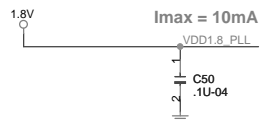
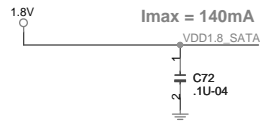
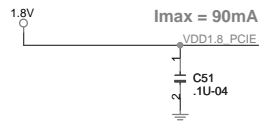
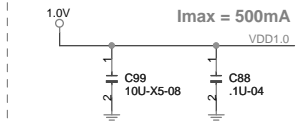
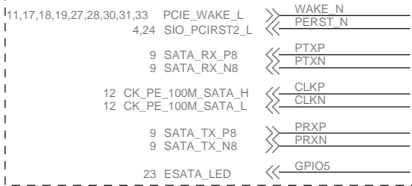
LAN\_HSOP/N請接到SB的PCIE RX端  
LAN\_HSIP/N請接到SB的PCIE TX端  
LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

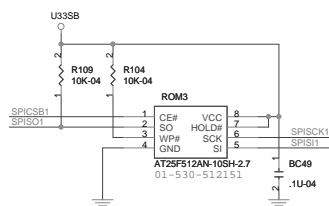
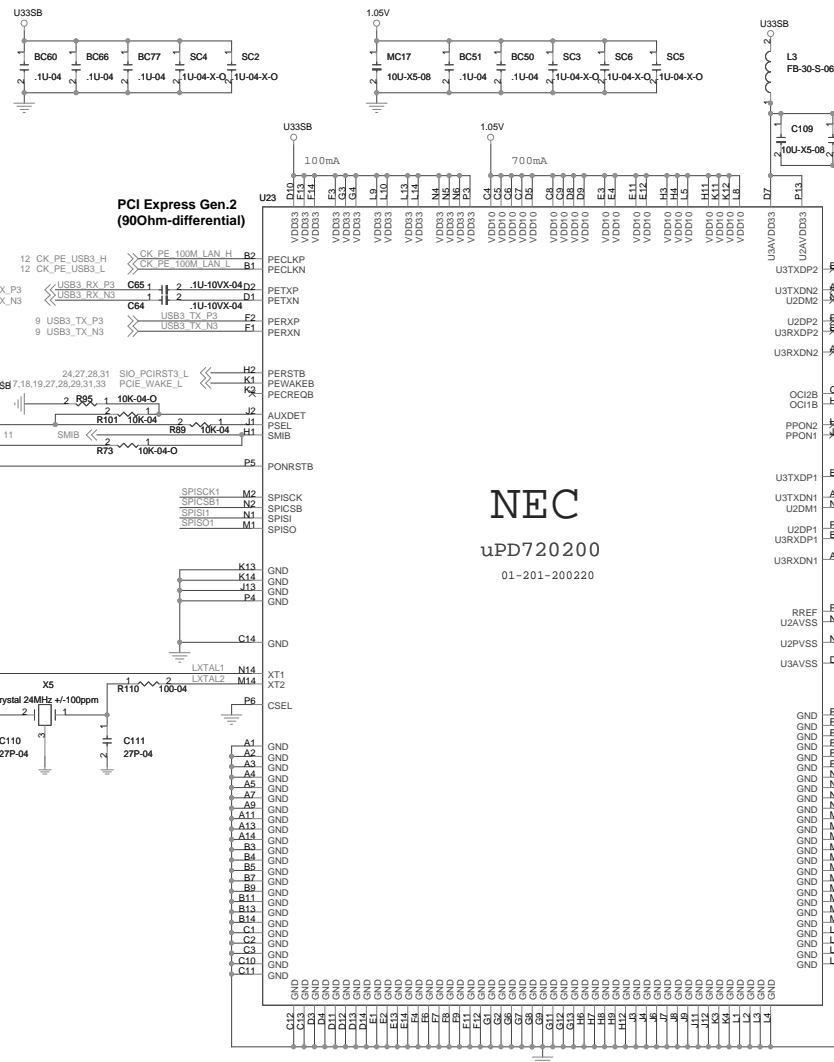


	RTL8111E-GR 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	decide by layout position USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-04
Cf		
Cg		

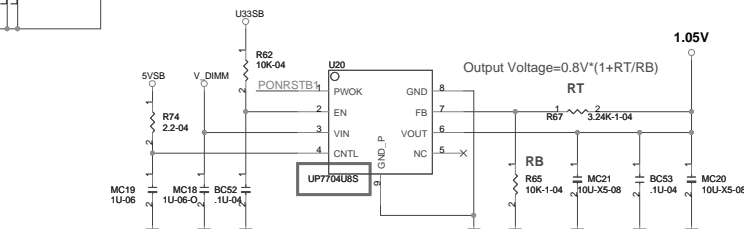


## External Connection





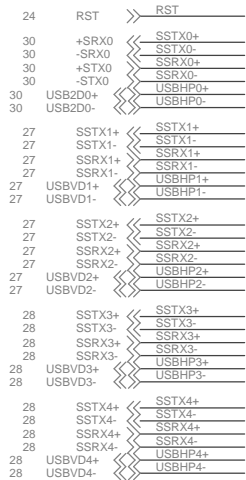
NEC  
uPD720200  
01-201-200220



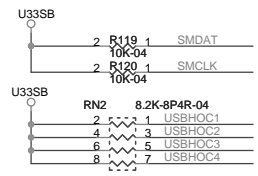
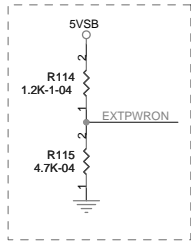
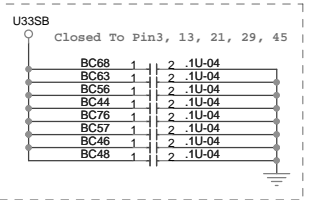
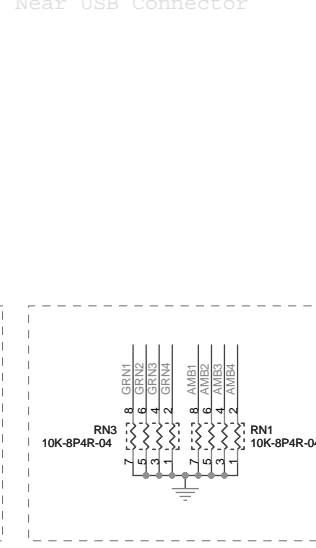
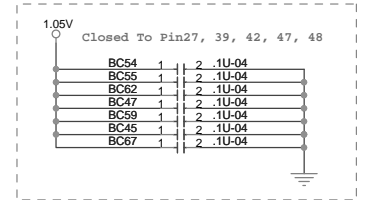
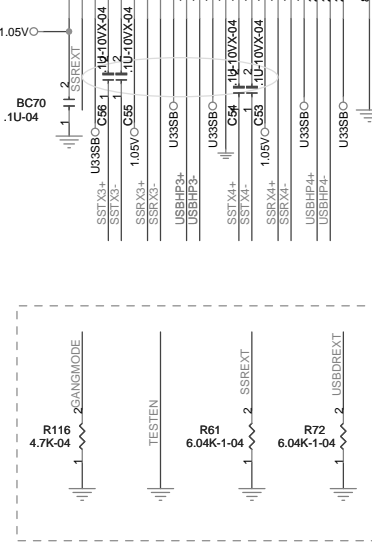
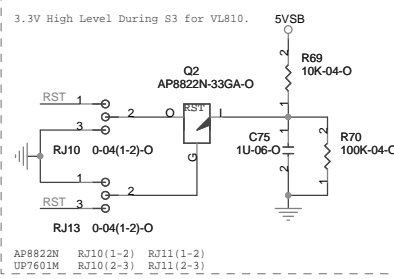
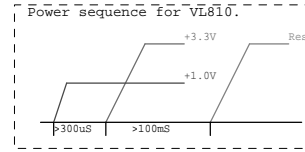
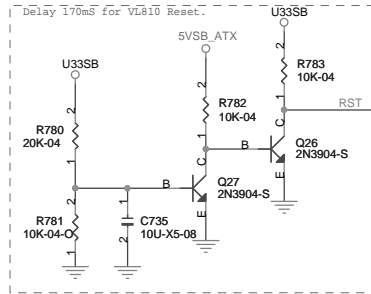
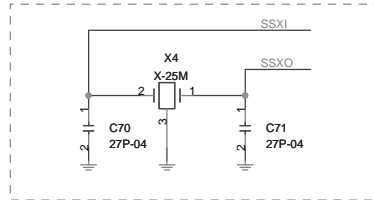
P-Package Pin to Pin Solution  
UP7704U8 -> 2A  
UP7706U8 -> 3A  
APL5910KAI -> 1A  
APL5920KAI -> 2A



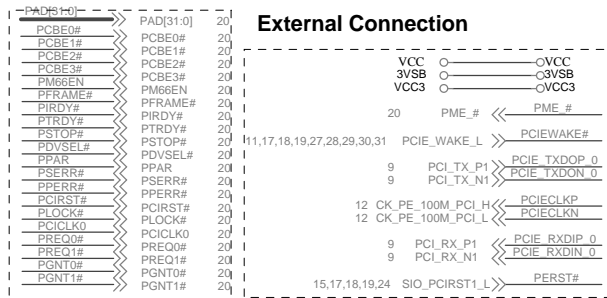
## External Connection



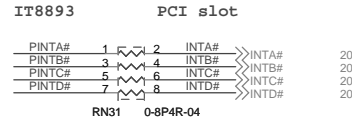
新手提醒：  
LAN\_HSOP/請接到SB的PCIE RX端  
LAN\_HSIP/請接到SB的PCIE TX端





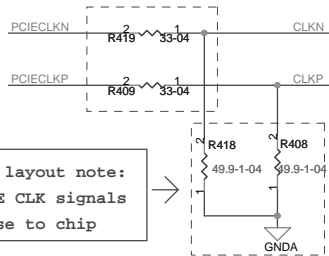


PCB layout note:  
Connect to PCIE  
PERST# Signal

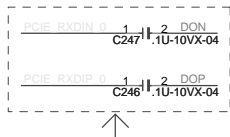


## COMMON

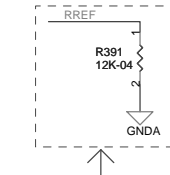
PCB layout note:  
PCIE CLK signals  
Close to chip



PCB layout note:  
PCIE CLK signals  
Close to chip



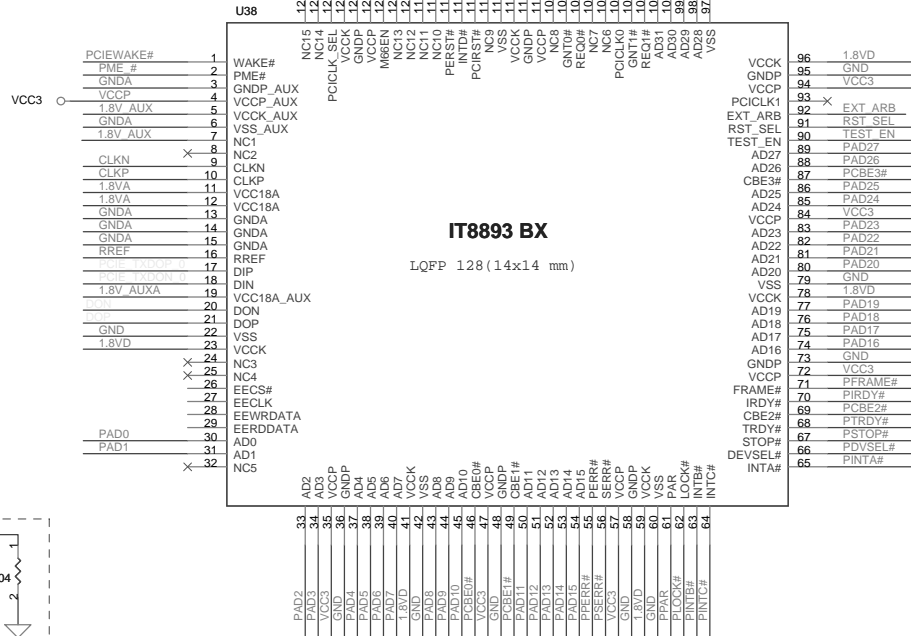
PCB layout note:  
PCIE TX signals  
Close to chip



PCB layout note:  
Close to chip

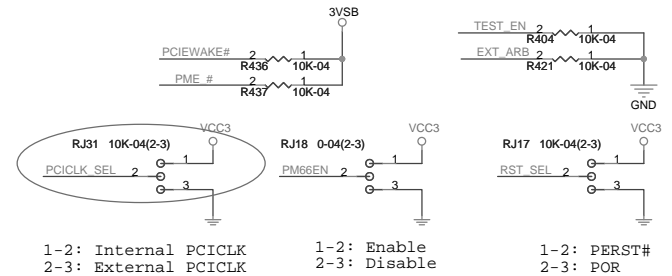
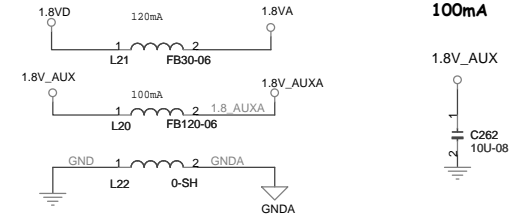
**PCIE DIP;DIN;DOP;DON PCB layout note:**  
To meet Differential Impedance :85 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
PCIE DIP and DIN trace width:9.5 mils  
PCIE DOP and DON trace width:9.5 mils  
Space between DIP/DIN and DOP/DON:14.5 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 2 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inchs (Max.)

**PCIE CLK PCB layout note:**  
To meet Differential Impedance :100 ohm +/- 15%  
To meet Single-ended Impedance :50 ohm +/- 15%  
CLKP and CLKN trace width:7 mils  
Space between CLKP and CLKN:14 mils  
L1 & L2 height:5 mils  
The signal traces Number of vias: 4 (Max.)  
The signal trace above analog GND plane  
Spacing from other groups:>25 mils  
Total trace length: 12 inchs (Max.)



## PCIE BUS 3.3\_AUX Power

## 1.8V\_AUX Power source



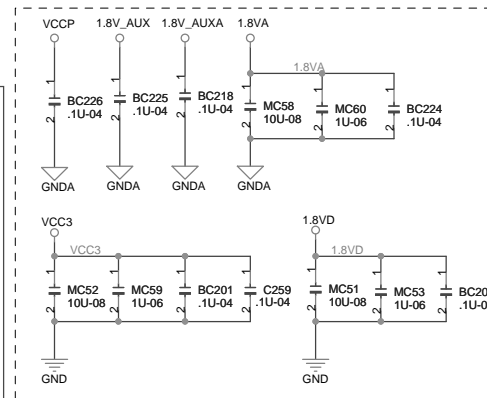
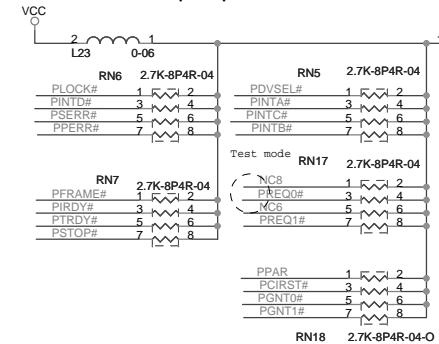
1-2: Internal PCICLK  
2-3: External PCICLK

1-2: Enable  
2-3: Disable

1-2: PERST#  
2-3: POR

## PCI BUS 5V external pull up

## PCI BUS 3.3V external pull up



# VCCSA Sequence

## System Agent core

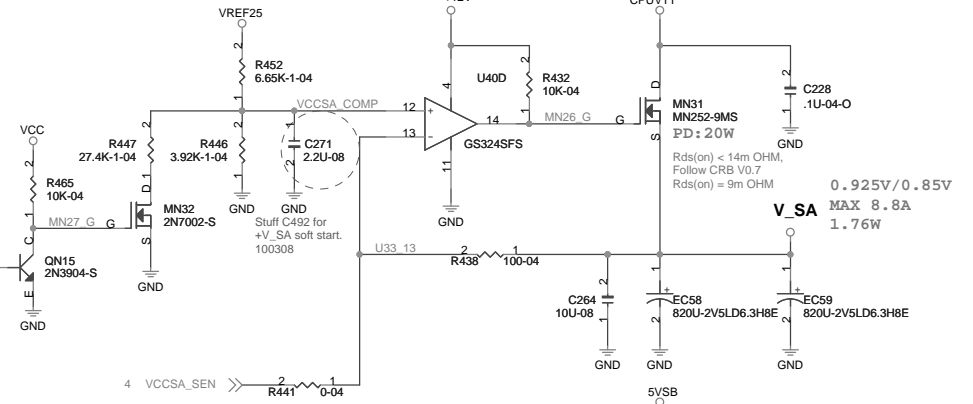
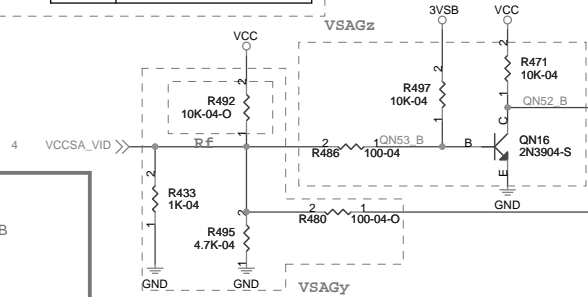
Default Stuffed:

Stuff VSAGz

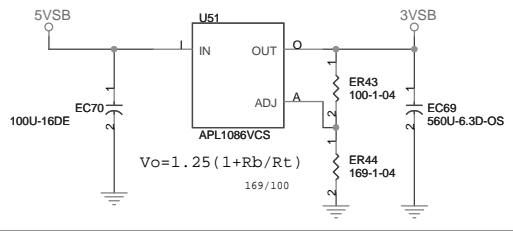
VCCSA voltage selection	
VID	V_SA
0	0.925V
1	0.85V

Stuff VSAGy

VCCSA voltage selection	
Rf	V_SA
unstuff	0.85V
stuff	0.925V



## +PS\_3VSB Circuit



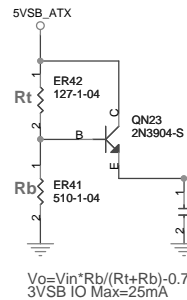
3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

H/W Monitor :1.05V (Traget)

GP26	GP27	PLL
1	1	1.83V
1	0	1.93V
0	1	2.02V
0	0	2.13V

## 3VSB\_IO



$$V_o = V_{in} \cdot R_b / (R_t + R_b) - 0.7$$

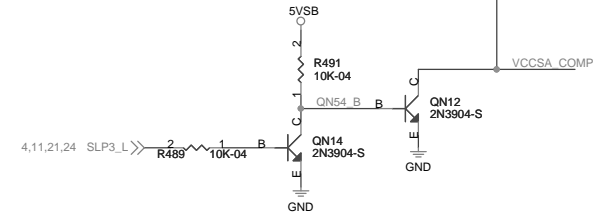
3VSB IO Max=25mA

H/W Monitor :1.05V (Traget)

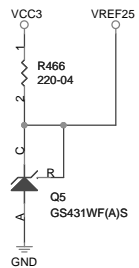
GP24	GP25	PCH
1	1	1.08V
0	1	1.13V
1	0	1.18V
0	0	1.23V

## PCH Core 1.05V

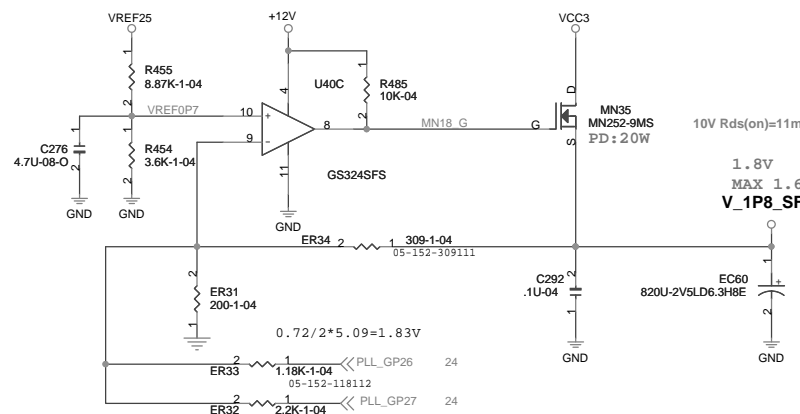
For V\_1P05\_PCH 1.05V/7.5AGND  
For V\_1P05\_ME 1.05V/2.5A



## VREF25

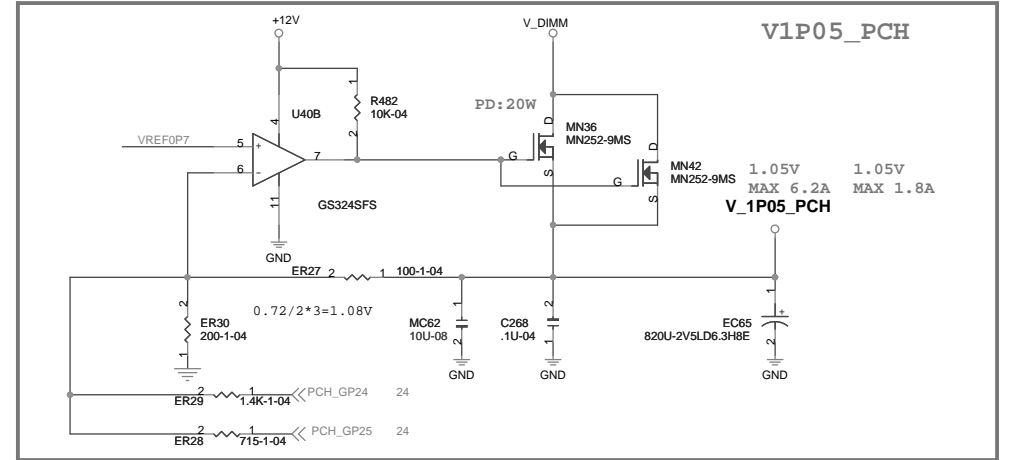


## V1P8\_SFR(1.6A max)



10V Rds(on)=11m  
1.8V  
MAX 1.6A  
V\_1P8\_SFR

## V1P05\_PCH



1.05V  
MAX 6.2A  
V\_1P05\_PCH  
1.05V  
MAX 1.8A



Elitegroup Computer Systems

Title		VCCSA, V1P05_PCH, V1P8_SFR
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$$V_{\text{DIMM}} = 0.8V * (1 + R_T / R_B)$$

RT8116A

COMP

C626  
27P-04-O

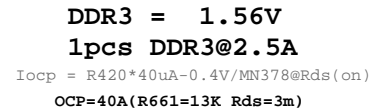
R734  
4.7K-04-O

C734  
33N-10V-04-O

LGATE

ER79  
15K-1-04-O

R740  
0-04-O

[illegible]

**VCC\_DUAL**

3VSB

R662 4.7K-04

B

Q7 2N3904-S

R658 4.7K-04

DUAL N

MN41 MN252-9MS

VCC

R649 1K-04

5VSB

R660 4.7K-04

3VSB

R648 4.7K-04

B

Q6 2N3904-S

R654 0-04

DUAL P

MN40 APM2301AAC

5VSB

C387 .01U-04-O

24 -3VSBWS

**VCC\_DUAL FOR V\_DIMM、USB3**

3VSB

DUAL P

DUAL N

VCC3

MS1

AO4609-S

U33SB

R146 2.2K-04-O

EC27 100U-16DE

3VSB

DUAL P

DUAL N

VCC3

MS2

AO4609-S

U33SBF

R565 2.2K-04-O

EC67 100U-16DE

V\_DIMM

R634  
10K-1-04

DDR\_VTT VREF

R633  
10K-1-04

C375  
1U-06

V\_DIMM

U54  
APL5336KAI-TRGS

1 VIN  
2 GND  
3 REFEN  
4 VOUT

8 Vcntl  
7 Vcntl  
6 Vcntl  
5 Vcntl

VCC

0.75V  
MAX 1A

DDR\_VTT

C384  
10U-08

C374  
1U-04

C334  
10U-X5-08

C382  
10U-X5-08



Title			
VDIMM, DDR_VTT, 5VDUAL			
Size Custom	Document Number		Rev
	P67H2-A		1.1
Date:	Wednesday, September 15, 2010	Sheet	35 of 42

## External Connection

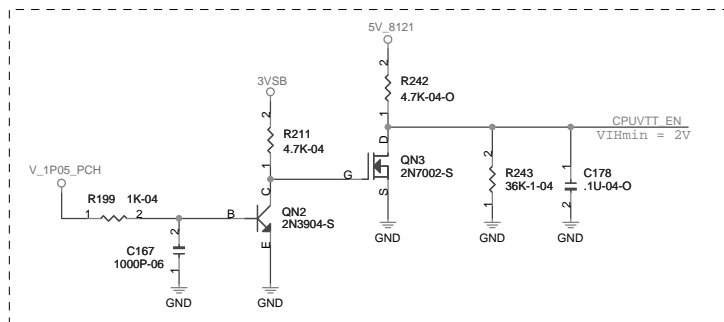
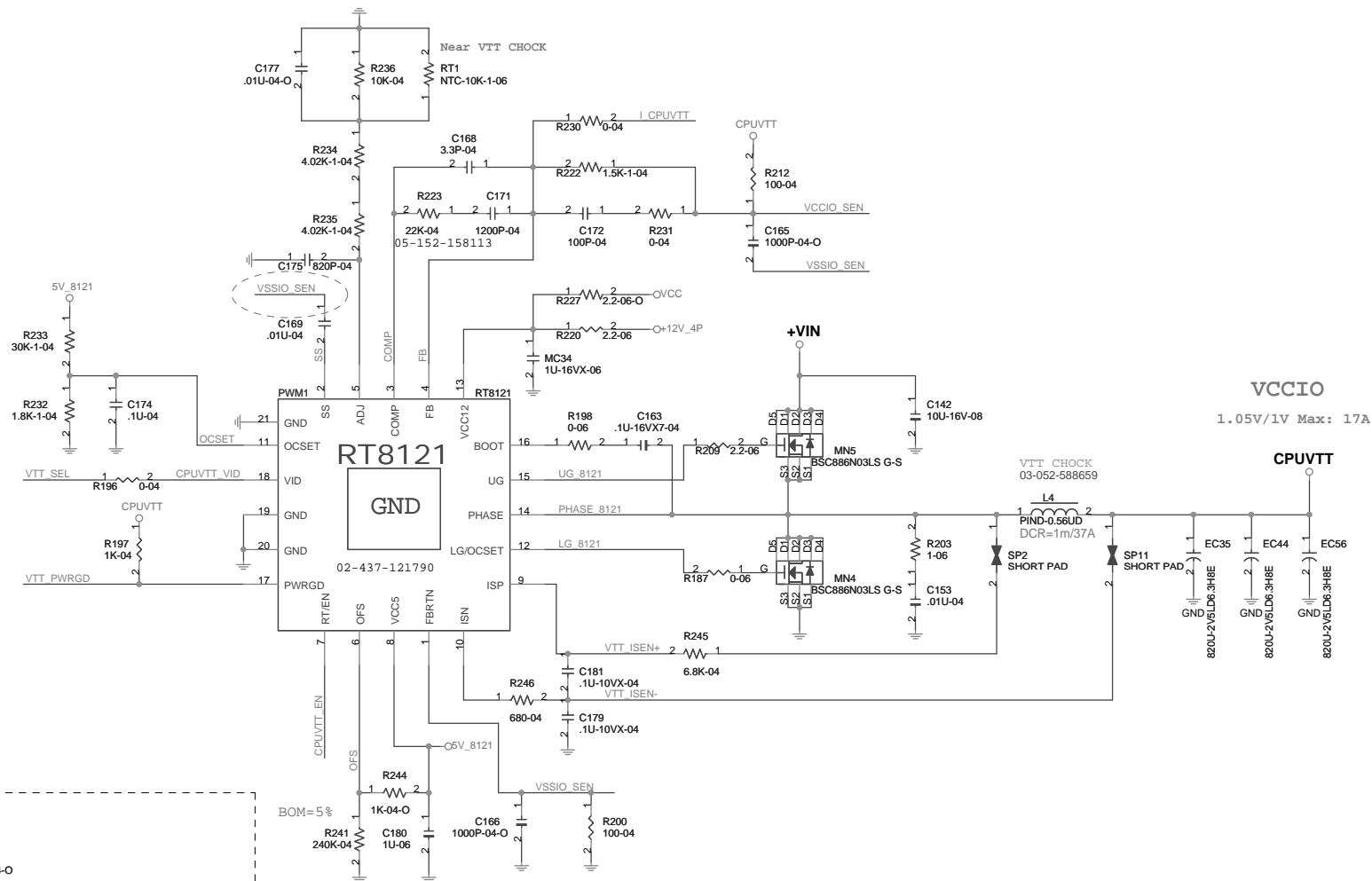
The diagram illustrates the external connections for the VCC, 12V, 3VSB, 5VSB, V\_1P05\_PCH, CPUVTT, and OCPVTT pins. The connections are as follows:

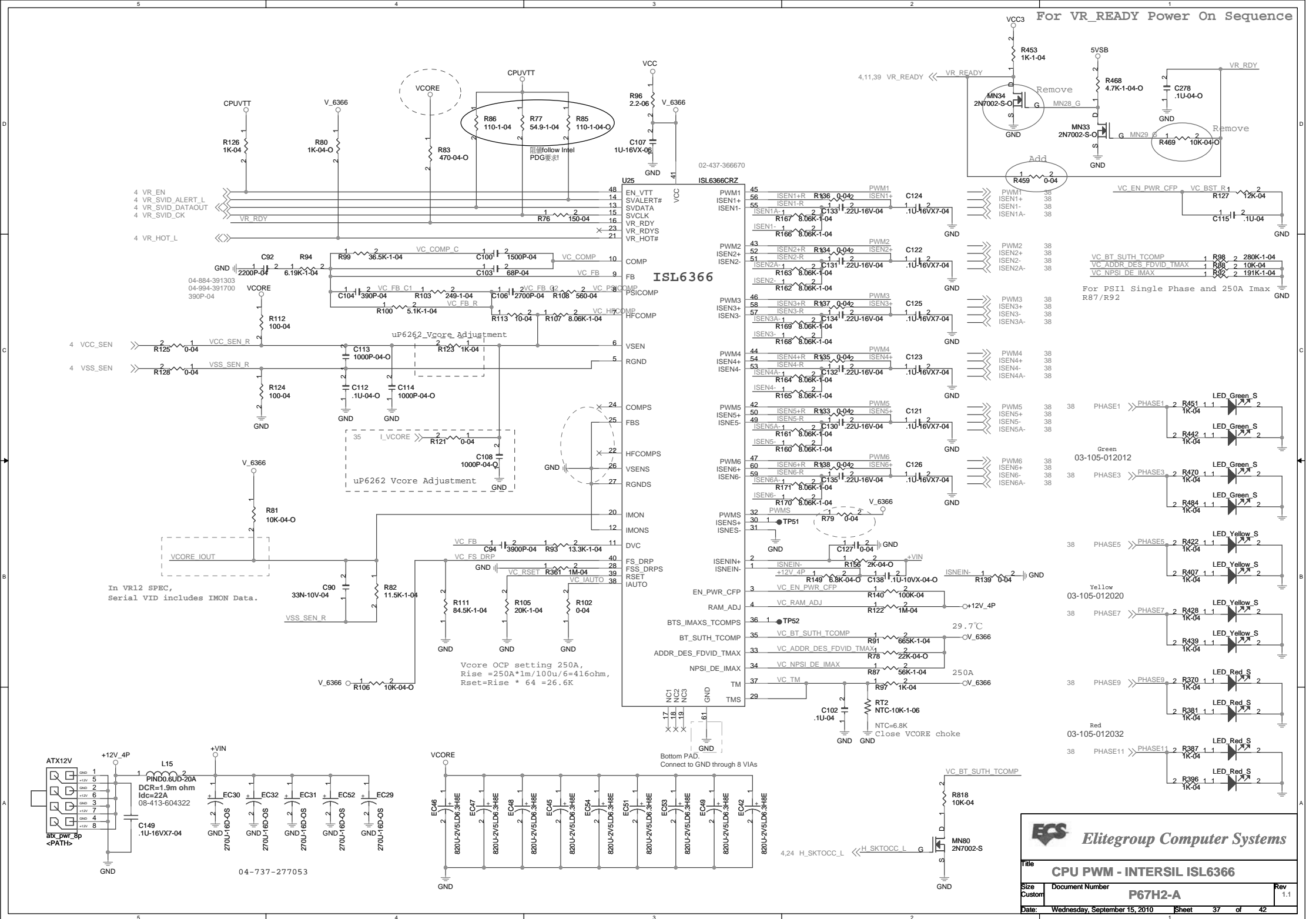
- VCC is connected to O\_VCC.
- +12V\_4P is connected to O+12V\_4P.
- 3VSB is connected to O3VSB.
- 5VSB is connected to O5VSB.
- V\_1P05\_PCH is connected to O\_V\_1P05\_PCH.
- CPUVTT is connected to OCPUVTT.

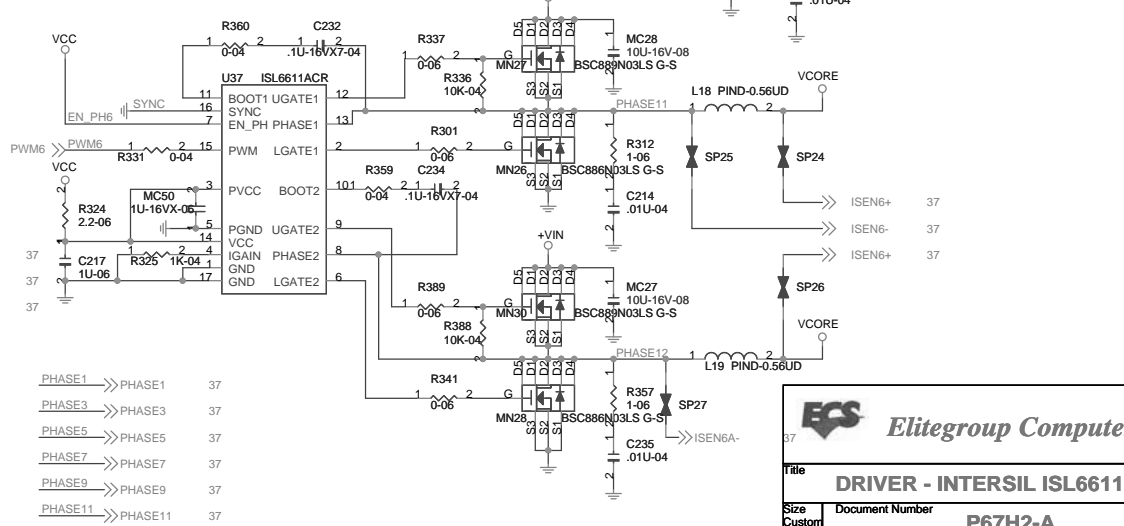
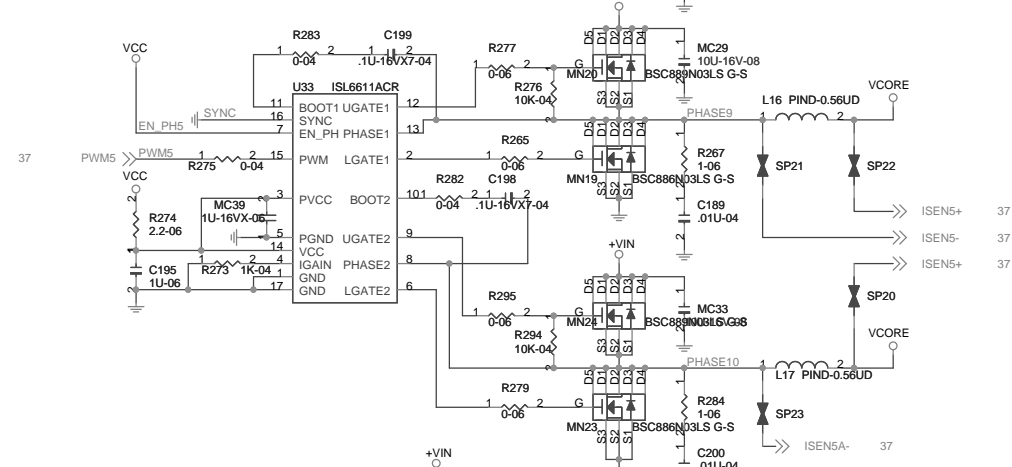
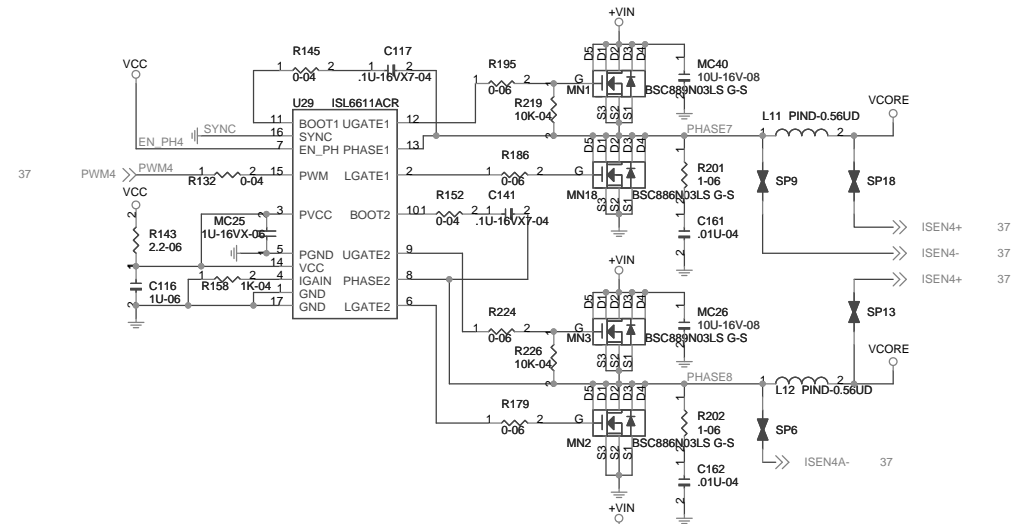
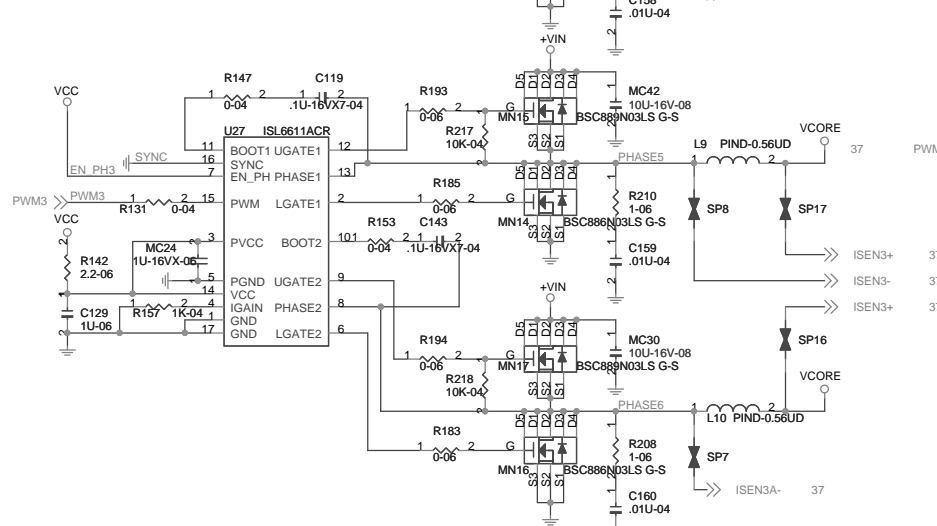
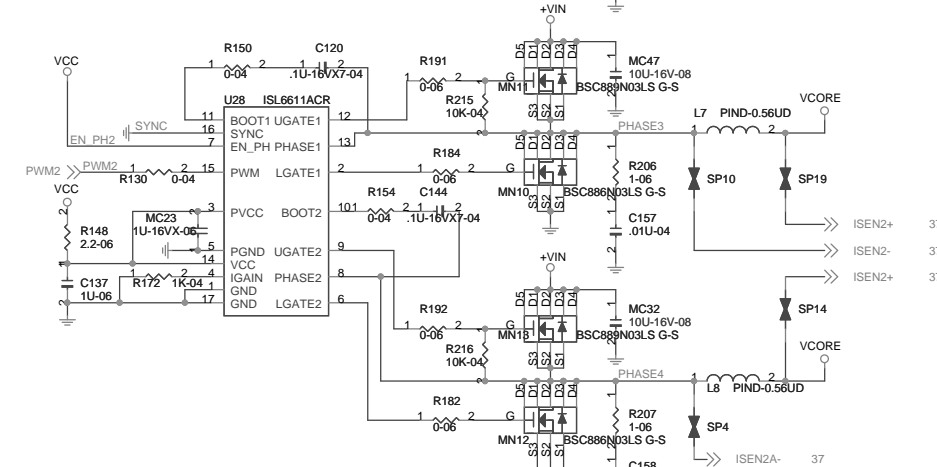
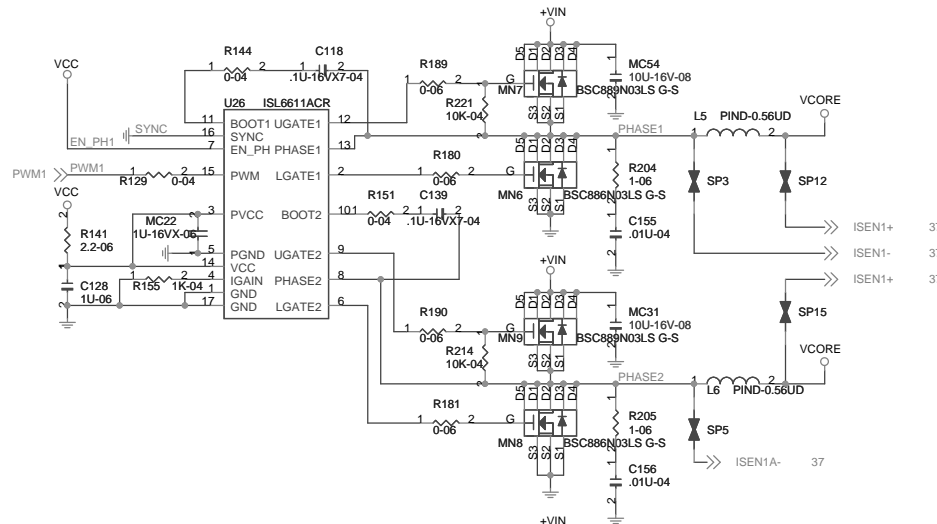
Below the main connection diagram, there are four additional connection points, each with a pin number and a label:

- 4 VTT\_SEL<< VTT\_SEL
- 34 VTT\_PWRGD<< VTT\_PWRGD
- VCCIO\_SEN VCCIO\_SEN
- 4 VSSIO\_SEN VSSIO\_SEN
- 35 I\_CPUVTT I\_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V







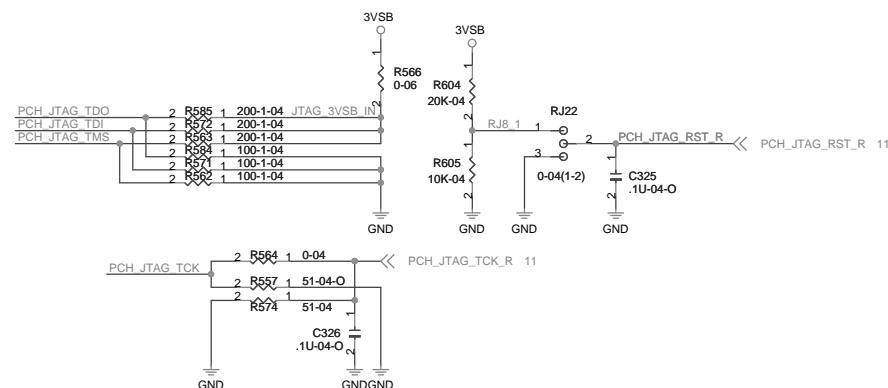
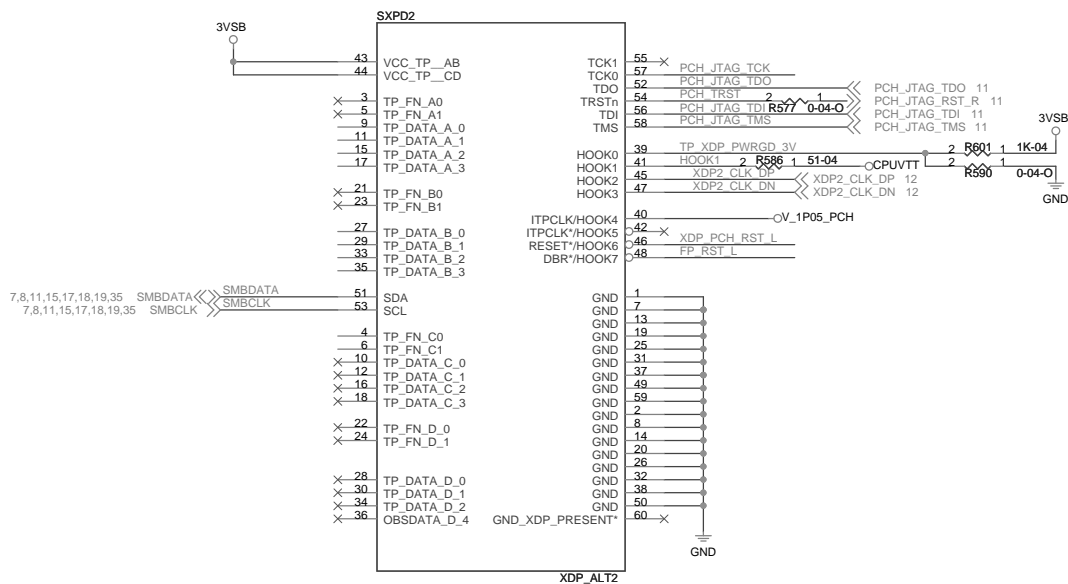
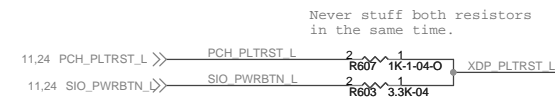
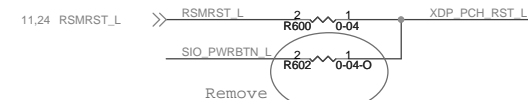
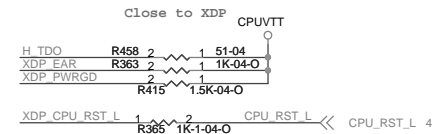
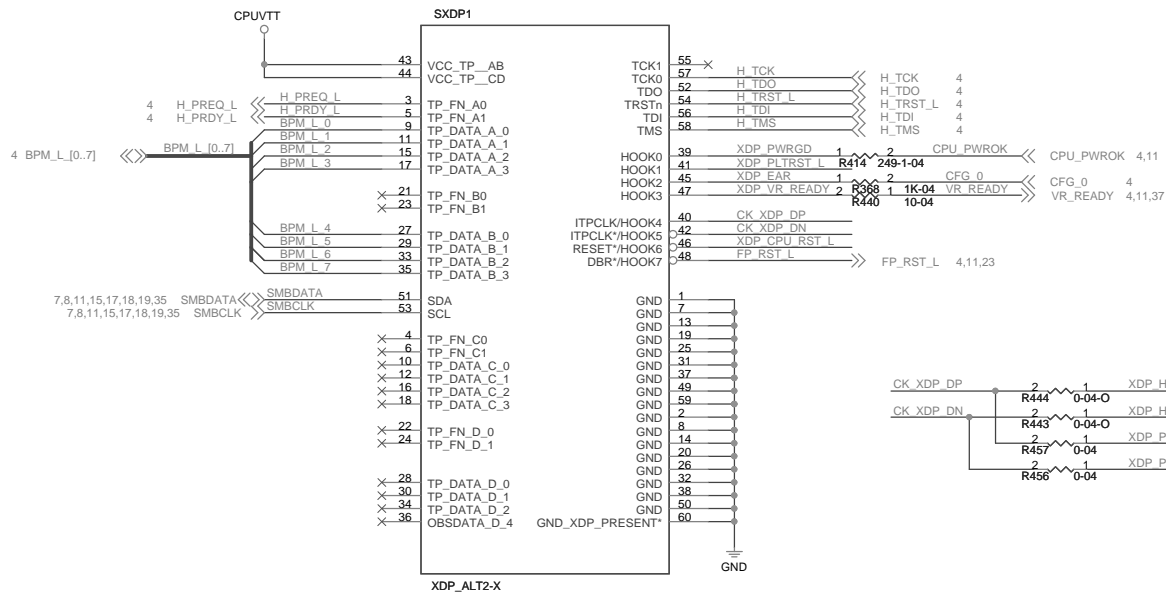
PHASE1 >>> PHASE1 37  
 PHASE3 >>> PHASE3 37  
 PHASE5 >>> PHASE5 37  
 PHASE7 >>> PHASE7 37  
 PHASE9 >>> PHASE9 37  
 PHASE11 >>> PHASE11 37


**Elitegroup Computer Systems**

**DRIVER - INTERSIL ISL6611**

Size Custom Document Number **P67H2-A** Rev 1.1

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DESIGN NOTE:  
PCH JTAG

DESIGN NOTE:  
DEFENSIVE DESIGN

ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P
12V +/-5%

Switching ISL6366 12 phases
-----------------------------------

Switching RT8121 1 phase
--------------------------------

Switching RT8105
---------------------

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0 1.0A_S3
V_SM_VTT	1.0A_S0

Linear LM324
-----------------

LDO APL5336
----------------

Linear LM324
-----------------

Linear LM324
-----------------

Intel Sandy Bridge CPU		
VCCP	VID 0.25~1.52V	85A , ICCMAX 112A
VAXG	NA	NA
VCCIO	1.05V(1V)	17A(IImax)
VCC_SA	0.925V(0.85V)	8.8A(IImax)
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLL	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

Fans
12V_200mA

SPI
VCC3_30mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

LUCID LT24102		
2.5VL	3.3V	1.3A
1.5VL	3.3V	1.7A
1.0VL	3.3V	4A

LDO APL5336
Switching RT8105
Linear LM324

Battery 3V
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LAN Realtek RTL8111E		
VDD3P3	3.3V	90mA
AVDD10	1.05V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8728		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC892		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

**Elitegroup Computer Systems**

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X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

SVDUAL Switch IC UP7536
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USB X4 Header	
VDD	5VDual 2.0A

USB X4 IO	
VDD	5VDual 2.0A

PS/2	
5VDual	1.0A

3VSB
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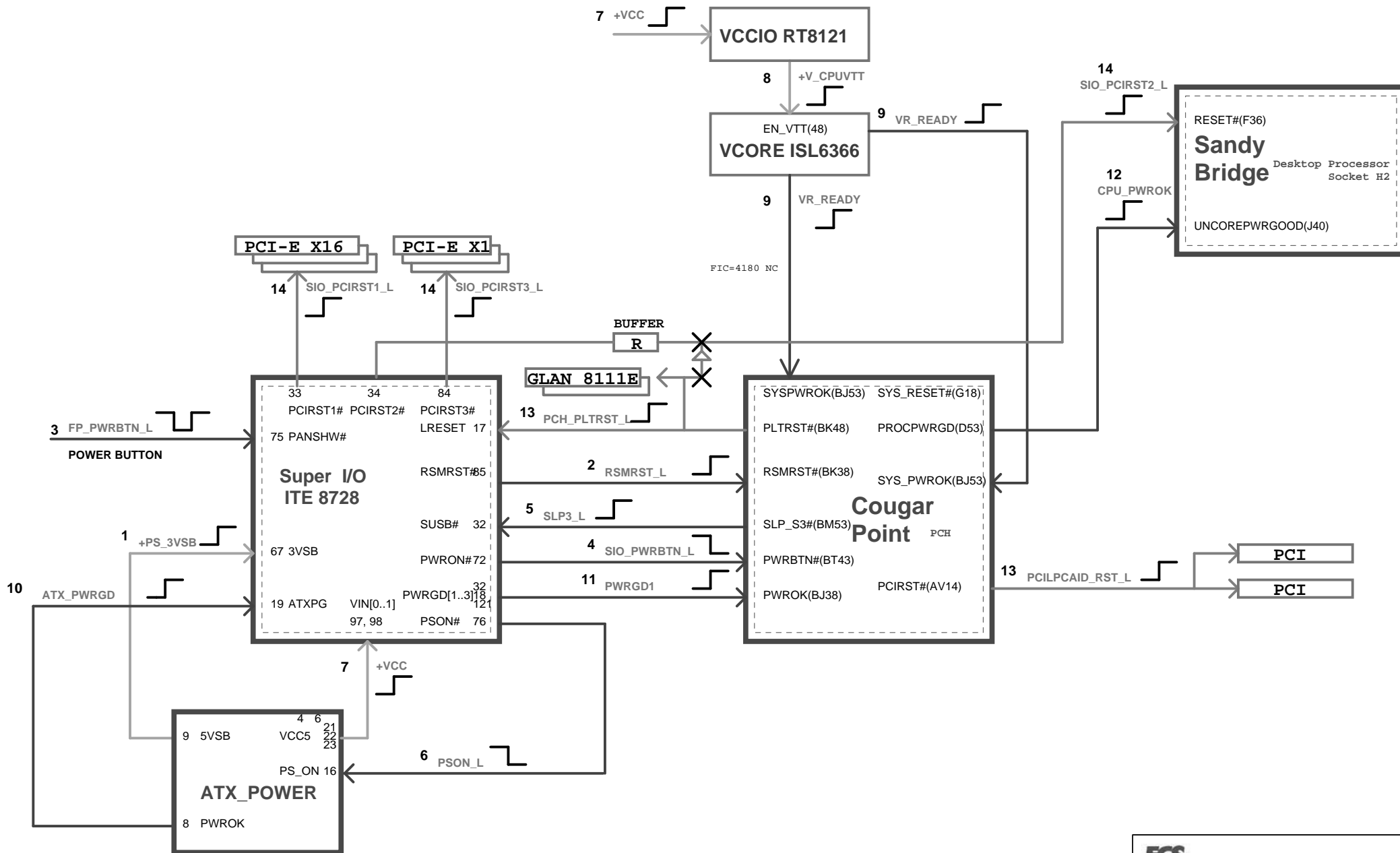
VCC3
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12V
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LDO
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5V
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# NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

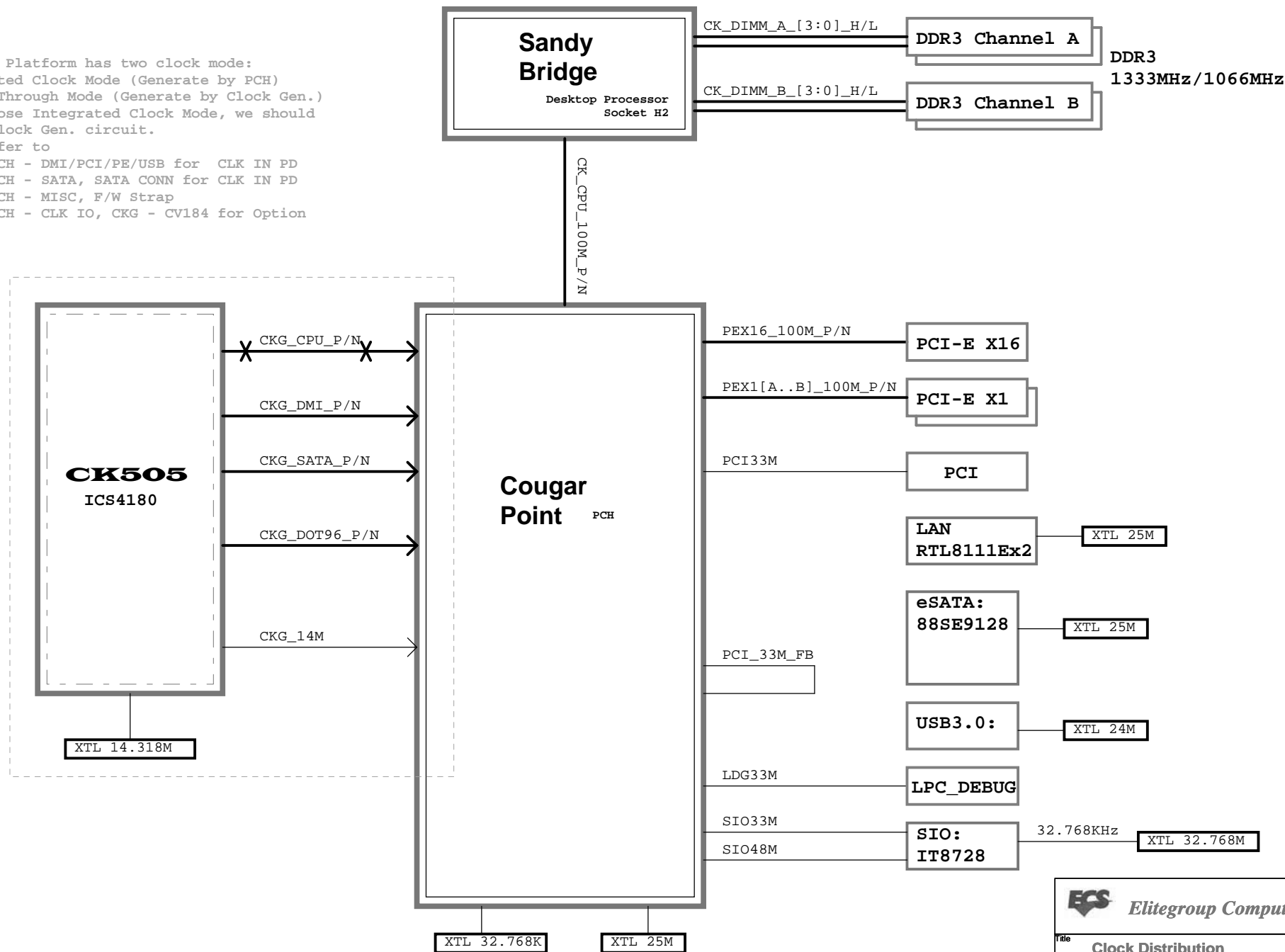
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



**ECS** Elitegroup Computer Systems

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